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## Effect of polishing pad with holes in electro-chemical mechanical planarization

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#### A R T I C L E I N F O

ABSTRACT

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Keywords: ECMP Polishing pad with hole WOD (wafer overhang distance) ECA (electric contact area) Material removal rate (MRR) profile Within wafer non-uniformity (WIWNU) Electro-chemical mechanical planarization (ECMP) process dissolves copper ions electrochemically by applying an anodic potential on the copper surface in an aqueous electrolyte, and then removes a copper (Cu) complex layer by the mechanical abrasion of a polishing pad or abrasives in the electrolyte. The ECMP process is a low pressure polishing method for metals such as copper, aluminium (AI) and tungsten (W) on dielectric materials such as silicon dioxide, low-k (LK) and ultra low-k (ULK) dielectrics, comparing to the amount of defects by the traditional Cu chemical mechanical planarization (CMP). The polishing pad used in the ECMP process is a conventional closed cell type pad (IC 1400 K-groove pad) with holes. It supplies the aqueous electrolyte to the copper surface and removes the copper complex layer. The material removal rate (MRR) and MRR profile were simulated and tested according to the changes of the wafer overhang distance (WOD) from the platen and the electric contact area (ECA). In order to derive the design rule of the system, the experimental results are compared with the simulation results. After the ECMP process, it was verified that the within wafer non-uniformity (WIWNU) was lower than 2% using the relatively uniform ECA pad (C-type) under the smallest WOD condition. The experimental results well matched the simulated results.

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#### 1. Introduction

Copper (Cu) is a superior material because of its higher electromigration (EM) [1] resistance and electrical conductivity, and has been recently used as one of the interconnect materials in semiconductor fabrication [2–4]. But, because Cu can be hardly etched by plasma and other methods, the dual damascene process was introduced for Cu removal and planarization [5-7]. The dual damascene process is a variation of the damascene whereby intersecting troughs in the same inter layer dielectric (ILD) are sequentially etched and concurrently backfilled with a metal stack. The trough overfill is then polished back to a planar surface by the chemical mechanical planarization (CMP) process, leaving an inlaid metal trace. Although the CMP process is a powerful polishing method, it generates many defects such as Cu dishing [8,9], erosion [8,9], metal delamination [10-12] and peeling [12,13] in the multi-metallization. And, generally in the case of a high step height, the Cu CMP process shows high material removal rate (MRR). If MRR is increased in the CMP process for planarization, the within wafer nonuniformity (WIWNU) becomes worse by the bending of the polishing pad in the high pressure condition [14–16] and the strong chemical effect in a slurry [17,18]. Furthermore, delamination can be generated at the interface of the Cu and dielectric materials,

resulting from the high pressure in the Cu CMP process. The yield of a semiconductor device is strongly affected by these defects generated in the CMP process. Therefore, the low pressure CMP is needed to minimize these defects [19]. However, the low pressure CMP process requires a long polishing time, costly equipment, high cost of consumables (CoC) and cost of ownership (CoO), and frequent replacement of chemicals and parts [20]. The demerits gave an opportunity to new process which is electro-chemical mechanical planarization (ECMP) process to solve the technical problems in the Cu CMP process. The concept of ECMP process is based on mechanical abrasion and the electrochemical actions of dissolution and the generation of a complex layer under a low pressure condition [21,22]. In the ECMP process, copper ions are dissolved electrochemically by applying an anodic potential on the copper surface in the electrolyte, and a solid copper on the Cu wafer surface changes to a Cu complex layer or passivation layer [23]. Next, the resulting copper complex layer or passivation layer is removed by the mechanical action of the polishing pad or the abrasive in the electrolyte [23]. Therefore, this process allows for the low pressure processing of copper interconnects built on mechanically fragile low-k dielectrics, whereas the traditional Cu CMP process of the high pressure condition does not [21,24–26]. So, the ECMP process allows fewer defects such as dishing, erosion, metal delamination and metal peeling than the traditional Cu CMP process [21,24-26]. Fig. 1 shows a schematic principle of the ECMP process. The polishing pad with holes helps the supply of the electrolyte to





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Fig. 1. The schematic principle of the ECMP process.



Fig. 2. The schematic and the development ECMP system; (a) the schematic of ECMP system, (b) the developed ECMP system.

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