Microelectronics Journal 42 (2011) 509–514

Contents lists available at ScienceDirect

Microelectronics Journal

journal homepage: www.elsevier.com/locate/mejo

RF model of flexible microwave single-crystalline silicon nanomembrane PIN diodes on plastic substrate

Guoxuan Qin [a,b,*], Hao-Chih Yuan [b], George K. Celler [c], Weidong Zhou [d], Jianguo Ma [a], Zhenqiang Ma [b,**]

[a] Tianjin University, School of Electronic Information Engineering, Tianjin 300072, PR China
[b] University of Wisconsin-Madison, Department of Electrical and Computer Engineering, Madison, WI 53706, USA
[c] Soitec USA, 2 Centennial Drive, Peabody, MA 01960, USA
[d] University of Texas at Arlington, Department of Electrical Engineering, Arlington, TX 76019, USA

ARTICLE INFO

Article history:
Received 1 September 2010
Accepted 18 October 2010
Available online 11 November 2010

Keywords:
Flexible PIN diode
Microwave
Modeling
Nanomembrane
Plastic substrate
Radio frequency (RF)
Single-crystalline silicon

ABSTRACT

This paper reports the realization and RF modeling of flexible microwave P-type-Intrinsic-N-type (PIN) diodes using transferrable single-crystalline Si nanomembranes (SiNMs) that are monolithically integrated on low-cost, flexible plastic substrates. With high-energy, high-dose ion implantation and high-temperature annealing before nanomembrane release and transfer process, the parasitic parameters (i.e. resistance, inductance, etc.) are effectively reduced, and the flexible PIN diodes achieve good high-frequency response. With consideration of the flexible device fabrication, structure and layout configuration, a RF model of the microwave single-crystalline Si nanomembrane PIN diodes on plastic substrate is presented. The RF/microwave equivalent circuit model achieves good agreement with the experimental results of the single-crystalline SiNM PIN diodes with different diode areas, and reveals the most influential factors to flexible diode characteristics. The study provides guidelines for properly designing and using single-crystalline SiNMs for flexible RF/microwave diodes and demonstrates the great possibility of flexible monolithic microwave integrated systems.

1. Introduction

There has been increasing enthusiasm on high performance, large-area flexible electronics for the past few years, because of their unique advantages such as bendability, light weight, and conformally attachable to any shape of surfaces [1]. Various applications are now employing the flexible micro- and macro-electronics, including large-area displays, electronic textile/paper, biomedical sensors, etc. [2–6]. Amorphous silicon, organics and polymers, and polycrystalline silicon are the most commonly used materials for the low-speed flexible electronics [1,4,6]. However, due to their poor crystalline quality and carrier mobility, these materials are not suitable for applications that require high-speed and high frequency operations, e.g. RFIDs, portable Wi–Fi devices, flexible airborne/space-borne communication systems, and surveillance and remote sensing radars [1,7]. Recently developed transferrable and flexible single-crystalline Si nanomembrane (SiNM), lifted from silicon-on-insulator: SOI wafers, makes fast electronics possible. The high carrier mobility of SiNMs, which is as high as their rigid bulk wafer counterparts [8–11], makes them promising for very high-frequency applications.

To transform the superior carrier transport characteristics of SiNMs into high-speed thin-film transistors (TFTs), we have developed a unique combined high-temperature and low-temperature process for transferrable SiNMs [11]. This led to the realization of microwave TFTs on a plastic substrate [11,12]. Other than active transistors, in order to build the flexible monolithic microwave integrated circuits, passive components that can be operated at RF/microwave frequency are indispensable. Furthermore, to accurately and efficiently design the flexible microwave integrated circuits, RF/microwave model of the PIN diodes is essential. However, all the available models for PIN diodes are based on bulky rigid wafers, accurate modeling of the novel microwave PIN diodes using single-crystalline SiNMs on plastic substrate is not yet reported.

There are two kinds of models commonly used: physical model and equivalent circuit model. Although a physical model can precisely predict single device 2D or 3D characteristics, it requires abundant numerical complexity [13], thus it is not suitable for circuit designs. On the other hand, an equivalent circuit model can provide sufficiently accurate performance at the device or circuit level, with much fewer model parameters and less computation

* Corresponding author at: Tianjin University, School of Electronic Information Engineering, Tianjin 300072, PR China. Tel.: 86 22 27408761.
** Also Corresponding author. University of Wisconsin-Madison, Department of Electrical and Computer Engineering, Madison, WI 53706, USA.
Tel./fax: 1 608 261 1095.
E-mail addresses: gqin@tju.edu.cn, guoxuanqin@hotmail.com (G. Qin), mazq@engr.wisc.edu (Z. Ma).

0026-2692/$ - see front matter © 2010 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mejo.2010.10.012

time. In this paper, we develop an RF/microwave equivalent circuit model for the microwave PIN diodes using transferable SiNMs on plastic substrate. The model provides guidelines for designing and using PIN diodes in flexible MMICs based on single-crystalline Si nanomembranes on plastic substrates.

2. Device fabrication

For the goal of flexible monolithic microwave integrated circuits, the fabrication process of the PIN diodes using transferable SiNMs on plastic substrate is fully compatible with that used to fabricate active transistors (TFTs) [11]. This process allows simultaneous fabrication of the active TFTs and passive PIN diodes on the same plastic substrate.

The process flow is briefly illustrated as shown in Fig. 1. The fabrication process begins with a lightly-doped p-type Si (0 0 1) SOI substrate with a 200-nm Si top layer and 200-nm buried oxide (BOX) layer. Align marks and the lateral n- and p-type regions were formed by optical photolithography. The patterned SOI sample then received ion implantation of phosphorus ions and boron ions, respectively, to form heavily doped n- and p-type regions. The sample was annealed at 850 °C for 45 min in N_2 ambient in a furnace (Fig. 1(a)). The well-controlled high-energy, heavily dosed ion implantation, and high temperature furnace annealing enable low contact and sheet resistance and thus low parasitic effects, which are the critical process steps to fabricate RF/microwave active and passive devices.

The 200-nm Si template layer was then patterned into strips or membrane with array of holes, followed by a plasma dry etching (SF_6/O_2) down to the BOX layer (Fig. 1(b)). After stripping off the photoresist, the sample was put into diluted hydrofluoric acid (HF) to etch away the underlying BOX layer and release the SiNMs weakly bonded on the Si handling substrate wafer via van der Waals forces (Fig. 1(c)) [14].

Then the sample was rinsed thoroughly with DI water and was subsequently brought face-to-face and firmly contacted with a ~175 μm thick polyethylene terephthalate (PET) substrate that was spin-coated with a SU-8 epoxy layer. Since the bonding force between the SiNM and the epoxy is stronger than the Si-to-Si bonding, the SiNM can be lifted off from the SOI substrate (Fig. 1(d)) and flip-transferred onto the PET substrate (Fig. 1(e)). This flip transfer technique makes the displacement of patterned Si-strips as small as possible after they were transferred onto the plastic substrate [12,15]. A UV exposure step was then used to cure the SU-8.

SiNMs were then selectively dry etched into smaller active area regions to further enhance the device flexibility. Finally, metal contacts and interconnects were formed by evaporating and a lift-off process (Fig. 1(f)). The highest temperature applied to the plastic substrates was kept below 120 °C.

The lateral arrangement of the PIN structure in this study has two major advantages: firstly, it allows simultaneous photolithography patterning and n-/p-type ion implantation for active TFTs and passive PIN diodes. Secondly, the lateral structure is not compromising the thinness of the SiNMs and thus device flexibility. The width of the I-region is determined by the distance between the p+ and n+ regions during photolithography. An I-region width of 2 μm is used in this study in order to achieve high-frequency response while maintaining proper breakdown voltages for power handling. The diode cross-section area can be calculated by multiplying the width of the p+ (or n+) region by the thickness of the

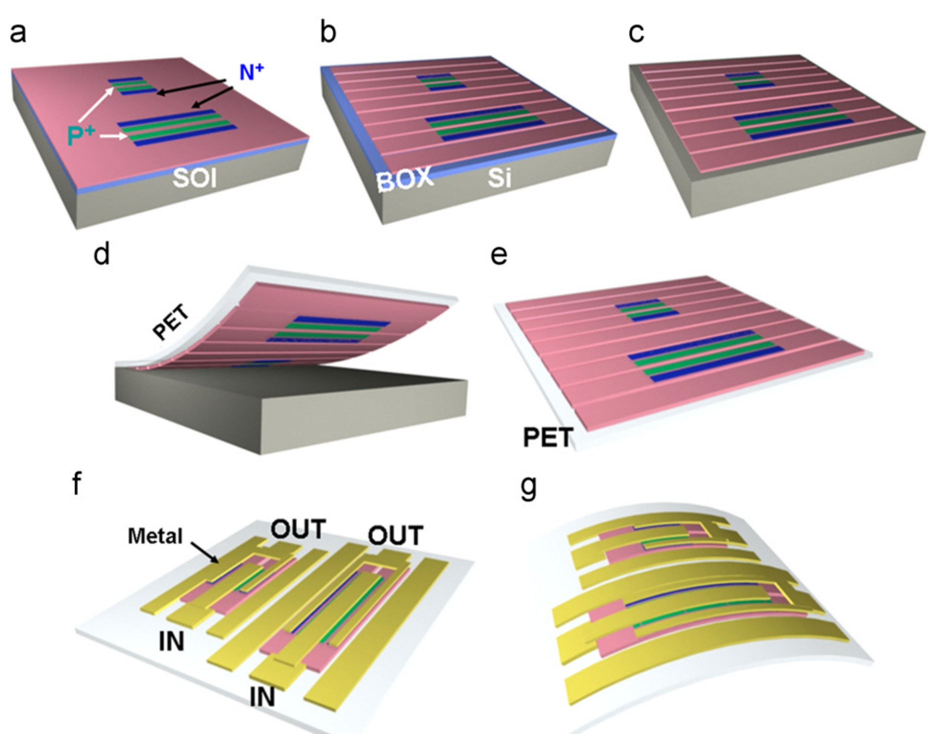

Fig. 1. Process schematic of fabricating flexible microwave single-crystalline Si nanomembrane PIN diode on plastic substrate (drawn not to scale). (a) SOI sample with heavily dosed n- and p-type regions by lithography patterning, ion implantation and high-temperature annealing. (b) 200 nm template Si layer is patterned into stripes and etched down to the buried oxide (BOX) layer by dry etching. (c) 200 nm single-crystalline Si nanostripes are released and attached on handling substrate wafer, by etching away the BOX layer in HF solution. (d) The Si nano-stripes (or SiNMs) are brought firmly contacted with PET plastic substrate with adhesive spinned SU-8 layer, and detached from the handling substrate. (e) The Si nano-stripes (or SiNMs) are flip-transferred onto the plastic substrate. (f) Finished flexible microwave PIN diode using transferable single-crystalline SiNMs on plastic substrate, after dry etching the SiNM active area and evaporating the metal connection and electrodes. (g) Illustration of the flexible single-crystalline SiNM PIN diodes under bending condition.