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RF MEMS capacitive switch on semi-suspended CPW using low-loss high-resistivity silicon substrate

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Abstract

A high capacitive ratio RF MEMS switch, with low-actuation voltage is designed, fabricated and experimentally validated on high-resistivity silicon (HRS) substrate. Thanks to very good fabrication control of all steps and to the high dielectric constant of TiO_2, a down/up capacitive ratio close to 200 is achieved with 8 V pull-in. It is also demonstrated that, using a passivated-surface HRS and semi-suspended conductors on air, the microwave losses in the CPW line are as low as 0.1 dB/mm at 20 GHz. The reported RF MEMS shunt capacitor is expected to serve as core device for phase shifting applications in the 10–20 GHz range, both for switching operations and as a variable capacitor in distributed MEMS transmission lines (DMTLs).
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1. Introduction

RF MEMS capacitors have been investigated for application in distributed MEMS transmission lines (DTMLs) phase shifters, both analog [1] and digital ones [2]. The idea is to periodically load a coplanar waveguide (CPW) with voltage-controlled varactors (two-state digital capacitors for digital DMTLs [2]), in order to tune the distributed capacitance, the phase velocity and the propagation delay in the line.

The first optimized loaded-line phase shifter was implemented using diodes [3]. However, diodes present low performances at high frequencies (RF), especially in terms of losses, tuning linearity and intermodulation distortion. RF MEMS capacitors overcome these problems, although, they might have limited tuning range and slower switching; however, these are not limiting factor for most phase shifter applications.

This paper addresses an electrostatically actuated RF MEMS capacitive shunt switch concept [4] (Fig. 1), which solves the limitations of functionality of digital capacitors [2] and adds two novel improvements: (i) under-etching of the substrate to reduce microwave losses and (ii) the use of titanium oxide (TiO_2), as dielectric ($\varepsilon_r = 20$), to achieve a high capacitive ratio at a low-actuation voltage.

This device enables the combination of high-performance RF MEMS switching capabilities (for signal routing in reconfigurable RF front-end systems [5] or switched-line phase shifters [6]) with the DMTLs tuning capacitors requirements.

2. Low loss substrate study: Under-etching process of surface-passivated high-resistivity silicon substrate (HRS)

There is a special need for careful selection of the substrate in RF operation, due to its determining influence on the losses. Quartz is commonly known as the ideal substrate at microwave frequency thanks to the fact that it is an insulating, and very low loss, material. The main disadvantage is its CMOS non-compatibility.

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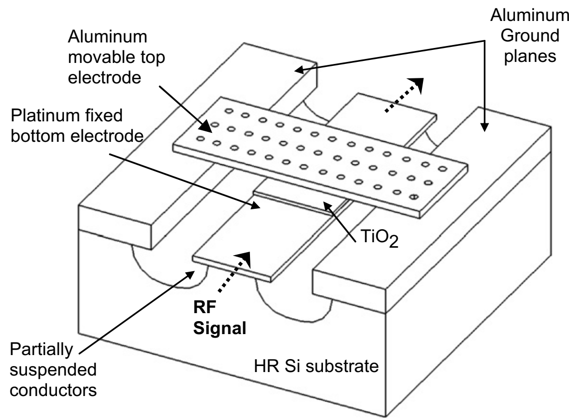


Fig. 1. Schematic view of the RF MEMS capacitive shunt switch.

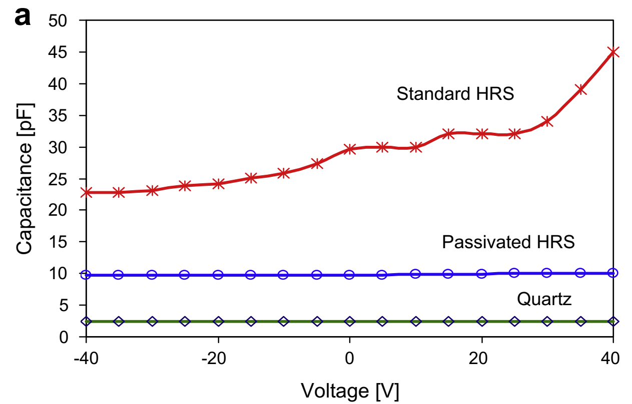
Concerning standard HRS substrates, a limitation is the non-negligible DC leakage current sensitive to DC bias, since HRS is not an insulating material [7]. Indeed, a silicon oxide (SiO_2) layer is placed between the substrate and the metallization. However, this results in the formation of an inversion layer of electrons in the Si–SiO_2 interface. This induced charge layer is voltage-dependent and increases microwave losses. To alleviate this problem, a highly defective Si as amorphous silicon (α-Si) can be grown on the Si surface, preventing the accumulation of electrons [8].

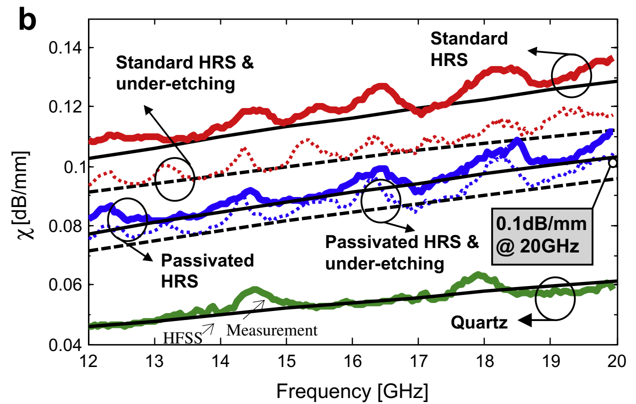
Fig. 2a shows that a DC bias affects the MOS capacitance on standard HRS, in contrast with quartz and passivated HRS, where no such effect is observed. This confirms the presence of charges at the interface of the standard HRS and shows the effectiveness of passivated HRS.

Fig. 2b shows simulated and measured microwave CPW losses on quartz, standard HRS and passivated HRS. Quartz substrate losses are negligible and measured losses can thus be attributed to the metal alone. This allows to extract the conductivity of the Aluminum (Al) CPW by comparison with Ansoft HFSS simulations (table in Fig. 2b). As the Al deposition method is identical for all substrates, its conductivity can be assumed to be the same.

Measured losses of standard HRS are much larger than simulated ones with the announced Si resistivity (10 kΩ cm). This phenomenon is linked with the formation of conductive surface channels at the Si–SiO_2 interface. In fact, measurements correspond to simulations with a Si resistivity of 0.7 kΩ cm, namely, 13 times lower. The passivated HRS significantly reduces the losses (Fig. 2b). Measurements now fit the simulations with the specified Si conductivity (10 kΩ cm), and hence demonstrates the validity of the passivation method.

Finally, to further reduce the microwave losses in the HRS substrates, an under-etching process was developed to realize semi-suspended conductors in air. In a CPW, most of the dielectric losses occur in the region close to the edges of the CPW, as a result of the large electric field density. Therefore, by etching the Si under the conductor, the substrate is replaced by an ideal dielectric, namely, air. First measurements results show the improvement obtained with a 4 µm-lateral air cavity (dashed lines in Fig. 2b).





Parameters	Ideal	HFSS simulation
1. Quartz → σ_{Quartz} → $\sigma_{Aluminum}$	0 S/m 3.7 10^7 S/m	0 S/m 3.2 10^7 S/m
2. Si-Standard HR → σ_{Si} → Resisitivity	0.01 S/m >10kΩ.cm	0.14 S/m 0.7kΩ.cm
3. Si-Passivated HR → σ_{Si} → Resisitivity	0.01 S/m >10kΩ.cm	0.01 S/m 10kΩ.cm

Fig. 2. (a) *C–V* curve measured at 1 MHz of the substrate MOS capacitors for Quartz, standard HRS and passivated HRS. (b) Losses measurements and Ansoft HFSS simulations of a CPW in: Quartz, standard HRS and passivated HRS before and after Si under-etching. The Table shows the ideal and simulated parameters in order to fit with the measurements.

Moreover, simulations indicate that further enlarging the air cavities would reduce the losses, eventually reaching those of quartz. Thus, under-etching of surface-passivated HRS substrate could become a close-to-ideal substrate for RF with minimum losses and all the well-known advantages of Si, especially when CMOS compatibility is required.

3. Fabrication process flow

The six-mask process described in Fig. 3 is used to fabricate the RF MEMS capacitive shunt switch using 10 kΩ cm P-type Si substrate. The process starts with 300 nm LPCVD α-Si passivation layer and 500 nm of sputtered SiO_2 as insulator.

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