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Compact small signal modeling and PSO-based input matching of a packaged CMOS LNA in subthreshold region

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Abstract

The paper reports a small-signal model of a cascaded, packaged, CMOS low noise amplifier (LNA) operating in subthreshold region. The proposed compact model has been verified through CADENCE simulations in standard 0.18 μm process. This model also accounts for the dominating role of some of the device parasitic capacitances in determining the input impedance of the amplifier. The closed form expression of the input impedance obtained-from this model is then used for synthesizing the input matching network of the common-source LNA using standard Q-based technique. It has been noted that the conventional Q-based matching approach does not provide symmetric matching characteristics (S_{11}) about the center frequency (900 MHz). To overcome this problem, a swarm intelligence-based evolutionary technique has been adopted for synthesis of the matching network. Symmetric nature is obtained both in terms of S_{11} as well as the real/imaginary parts of the input impedance.

Keywords: LNA; Subthreshold; Q-based matching; PSO

1. Introduction

CMOS low power radio frequency systems are being widely used in narrow-band, wireless embedded sensor applications [1,2]. To remain operative over long periods of time, these systems demand low-voltage and low-current operation. Several approaches have been adopted to reduce the power consumption. Among those, CMOS RF circuits operating in subthreshold region is a promising technique [3,4].

The large-signal behavior of MOSFETs in subthreshold region is well characterized by the standard exponential I–V relation. However, in high-frequency domain a compact small-signal model is necessary for system optimization and synthesis using closed-form expressions. In this paper, we present an analytical, compact small-signal model of a packaged low noise amplifier (LNA) operating in subthreshold region. It has been shown through extensive CADENCE SpectreRF simulations in standard 0.18 μm CMOS process that this model accurately captures the effects of the device intrinsic capacitances and the pad/pin parasitics, which play a dominating role in subthreshold region.

The pad/pin parasitics affect the input impedance of the LNA. In order to reduce this effect, separate off-chip π- or T-matching network is generally used for such amplifiers [5].

It has been observed that the standard Q-based matching technique [6] does not produce symmetrical matching over the frequency band (850–950 MHz). Therefore, in this paper a particle swarm optimization (PSO)-based evolutionary technique for the synthesis of π-matching network has been developed to provide more accurate matching.

The paper is organized as follows: in Section 2, an analytical compact small-signal model of a packaged inductive source degenerated cascode LNA is illustrated and a modified expression of input impedance is derived. Section 3 deals with, π and T impedance transformation techniques for Q-based single band input matching. In Section 4, a PSO-based algorithm is discussed for synthesis of input matching network. The paper is concluded in Section 5. Finally, the Appendix presents elaborate analytical derivations.

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2. Small-signal analysis of packaged low-noise amplifier

Accurate and efficient LNA input impedance modeling is essential for automated generation of the matching network and to understand the effects of several device parameters (g_m, W/L, C_{gs}, C_{gb}, C_{sb}, C_{jw}, etc.) on the input impedance in high-frequency operation. Especially for low-voltage, subthreshold region of operation, the effects of several parasitic device capacitances, which were originally neglected in the saturation region model [7,8], should also be included in the model.

A schematic of a packaged single-ended LNA is shown in Fig. 1, where Fig. 2 depicts its equivalent model.

Applying Kirchoff's voltage and current laws, on the above network, the input impedance, excluding the parasitic can be expressed as [see Appendix]

$$Z_{in1} = \left\{ \frac{Z^*}{1 + sZ^* C_{gd1}(1 - A^*)} \right\} || \frac{1}{sC_{gb1}} || R_{bias}, \tag{1}$$

where

$$Z^* = \frac{1}{sC_{gs1}} + \left\{ (R_{ss} + sL_s) || \frac{1}{sC_{sb1}} \right\} \left(1 + \frac{g_{m1}}{sC_{gs1}} \right), \tag{2}$$

$$\frac{V_0}{V_1} = A^* = \frac{-g_{m1}}{(sC_{total} + g_{m2})(1 + (sC_{gs1} + g_{m1})\{(R_{ss} + sL_s) || 1/sC_{sb1}\})}, \tag{3}$$

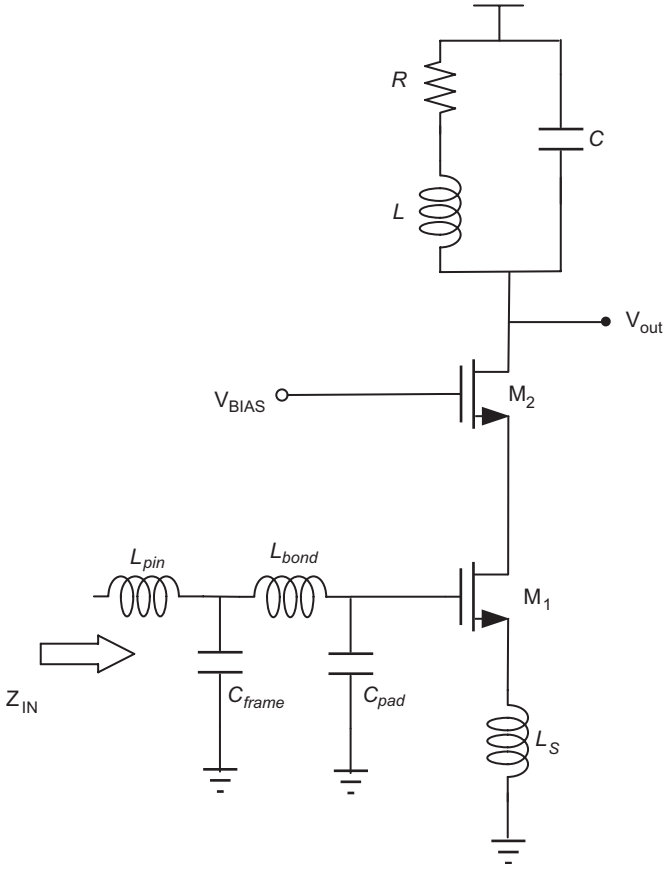

Fig. 1. Single-ended packaged cascode LNA (without input matching network).

where A^* is the gain from the gate terminal to the drain terminal. C_{total} is the cumulative sum of the capacitances C_{gs2}, C_{db1}, C_{sb2} and C_{jw}.

Hence, the cumulative input impedance, including the parasitic can be expressed as

$$Z_{in} = \left(sL_{bond} + Z_{in1} || \frac{1}{sC_{pad}} \right) || \frac{1}{sC_{frame}} + sL_{pin}. \tag{4}$$

Without the inclusion of C_{gb}, C_{sb} and C_{jw}, normally neglected in saturation region, the behavior of the small-signal equivalent model in subthreshold region, deviates much from the actual implementation (Fig. 3). In addition to these effects, the pad/pin parasitics substantially affect the input impedance of the circuit.

It has been verified through CADENCE simulation in 0.18 μm CMOS process that the behavior of the small signal equivalent model matches closely with that of the actual transistor-level implementation of the LNA (Fig. 4).

3. *Q*-based input matching

In GSM/ISM band receiver design, it is required to obtain a good input match not only at the carrier frequency (900 MHz/1.8 GHz) but also over a certain bandwidth around it. This is why a specified limit is set on reflection parameters (S_{11}, S_{22}) over the bandwidth of the LNA at input end.

It can be shown that the input impedance of a simple inductively degenerated LNA is

$$Z_{in} = \frac{g_m L_S}{C_{gs}} + sL_S + \frac{1}{sC_{gs}}. \tag{5}$$

Hence, by simply adjusting the values of g_m and L_S, one can obtain moderate input matching over the bandwidth. But, due to pad/pin parasitics, the input impedance of the LNA gets largely modified. Hence, this approach is unrealistic in packaged ICs. Therefore, a separate off-chip matching network is required in such cases. Several such matching networks can be found in the literature [5], but π and T matching networks provide good matching performance over the bandwidth with minimum number of components.

Conventional matching techniques are based on parallel–series impedance transformation at the desired frequency f_0. The negative (positive) imaginary part of the input impedance is then balanced by putting an inductor (L_{series}) (or a capacitor) in series (Fig. 5). This gives effectively, a real impedance part (R_P). After that, using a π- or T-matching network, the input impedance can be easily matched to 50 Ω.

As mentioned before, the input impedance of the cascoded LNA gets modified due to the pad/pin parasitic resulting in the reduction of the real part of the impedance. For this reason, a π-matching network is more suitable in this case as compared to a T-matching network.