

CMOS balanced regenerative frequency dividers for wide-band quadrature LO generation

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Abstract

CMOS regenerative frequency dividers, based on a fully balanced Gilbert cell, are analyzed in this paper for quadrature local oscillator (LO) signal generation. Driven in opposite phase by double frequency signals, they provide quadrature waveforms while simultaneously driving large mixers LO input capacitances, thereby avoiding power hungry buffers typically required. Experimental results, carried out on 0.18 μm CMOS prototypes, show 68% bandwidth around 2 GHz center frequency, with a quadrature accuracy better than 1° , making them suitable for multi-standard wireless receivers. To keep the output amplitude constant while simultaneously minimizing the average power consumption, a digital calibration loop regulates each divider biasing current.

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1. Introduction

CMOS technology is now mature for manufacturing transceiver circuits for several wireless communication applications [1]. The direct conversion receiver architecture is commonly recognized as the optimum choice for highly integrated solutions. Fig. 1 depicts a simplified block diagram showing the radio front-end (LNA and mixers) and the quadrature local oscillator (LO) generation circuits. Presently, there is a growing interest toward reconfigurable radios for multi-standard applications, able to handle as many communication standards as possible with maximum hardware reuse and minimum power consumption. In this framework, multi-standard receiver front-ends and LC tank voltage-controlled oscillators (VCO) with very wide tuning range were presented [2,3]. Wide-band dividers by 2, intended for I and Q LO

generation, are proposed in this paper. One of their main features is the high driving capability, particularly important when active mixers employing large area switching devices are used to minimize $1/f$ noise [4,5], leading to a large load capacitance (C_{LO} in Fig. 1, ranging from several hundred of fF to one or more pF) to be driven by LO waveforms.

The regenerative divider, reported in Fig. 2a, is based on a fully balanced multiplier (a Gilbert cell) and employs an LC resonant load. When compared to resistively loaded frequency dividers it allows considerable power consumption reduction since the capacitive load may be tuned-out by the tank inductors. When compared to conventional injection locked LC frequency dividers, recently proposed as a power saving solution and reported in Fig. 2b [6,7], it shows a larger operation bandwidth.

Prototypes, realized in a 0.18 μm CMOS, demonstrate an operation bandwidth as large as 68% around 2 GHz, while driving 1.5 pF load capacitance. Conventional topologies of injection locked frequency dividers with the same load would provide a maximum bandwidth of less than 10%. To stabilize the output amplitude variation versus

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frequency and simultaneously minimize the average power consumption, a digital calibration loop has been realized to adjust the divider biasing current from 2 mA at center frequency to 12 mA at band edge.

The paper is organized as follows: Section 2 reviews the fundamental mechanisms limiting the operation bandwidth of regenerative frequency dividers, thus highlighting the advantages of the proposed solution against injection locked oscillators. In Section 3, balanced frequency dividers are analyzed in detail providing useful design equations. Prototypes design and experimental results are discussed in Section 4 while Section 5 draws the conclusions.

2. Review of LC tank regenerative dividers

Injection locked oscillators and the divider discussed in this paper can be regarded as regenerative frequency

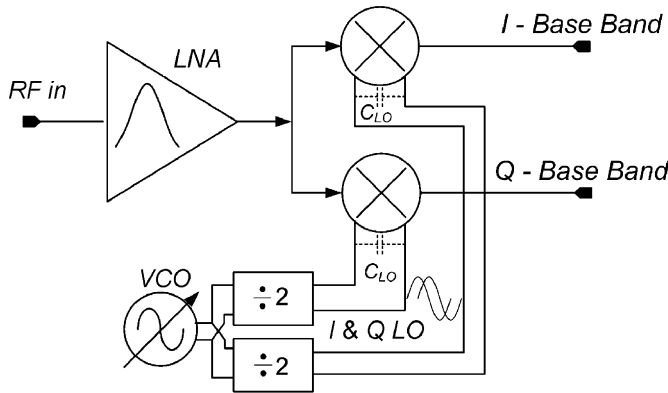


Fig. 1. Simplified block diagram of a direct conversion receiver showing the analog front-end (LNA and mixers) and the quadrature local oscillator generation system.

dividers [8]. Fig. 3 shows the behavioral block diagram. It consists of a feedback loop, with an analog multiplier driven by the output voltage, and an LC band-pass filter, tuned at half the input frequency, in the forward path. Intuitively the loop divides the input signal frequency because the fundamental component at the multiplier output (at half the input frequency) is transferred to the output while harmonics are filtered out by the selective load.

The difference between the two circuits of Fig. 2 consists in the adopted multiplier, i.e., single balance for the injection locked oscillator and fully balanced (made of transistors M_1 – M_6) for the alternative here discussed.

The multiplier input signal is comprised of a DC biasing component plus an injected signal at twice the output frequency in the conventional injection locked oscillator whereas the DC term is suppressed by the fully differential operation of the multiplier in the balanced divider. As a consequence, the circuit of Fig. 2a does not self-oscillate because the loop opens up (i.e., $I_{\text{TANK}} = 0$) when the input signal is not applied.

More important is the effect of the DC component on divider operation bandwidth. The LC filter has finite quality factor Q . Its impedance $Z(\omega)$ is approximated near resonance by

$$Z(\omega) \approx \frac{R_0}{1 + j2Q((\omega - \omega_0)/\omega_0)}, \quad (1)$$

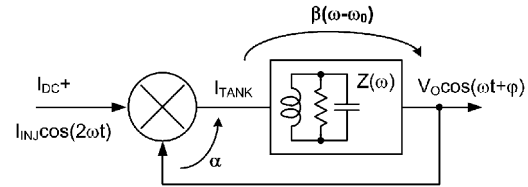


Fig. 3. Behavioral model of a regenerative frequency divider by 2.

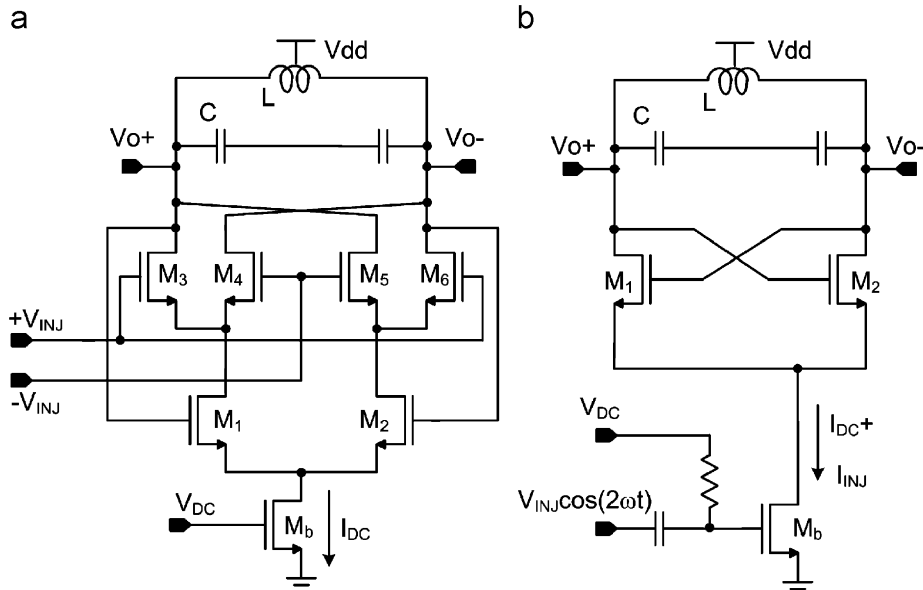


Fig. 2. Schematic of the balanced divider (a), second harmonic injection locked oscillator (b).

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