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A novel double RESURF LDMOS and a versatile JFET device used as internal power supply and current detector for SPIC

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Abstract

In this paper, a novel double RESURF LDMOS with multiple rings in non-uniform drift region is proposed and successfully fabricated. The proposed device maximizes the benefits of the double RESURF technique by optimizes key process and device geometrical parameters in order to achieve the lowest on-resistance with the desired breakdown voltage. In addition, a versatile JFET device is firstly developed. The JFET device cannot only be used as the current detector, but also be used as the internal power supply for SPIC. Besides, it is compatible with Bipolar-CMOS technology, without any additional processes required.

Keywords: RESURF LDMOS; SPIC; Current detector; JFET; Power supply

1. Introduction

Smart power IC (SPIC) combines the power device with CMOS logic and/or bipolar analog circuits on one chip are gaining more and more attentions, such as motor control, electronic ballasts, and switched mode power supplies. The integration of discrete elements promises to provide improved performance, increased functionality, enhanced reliability and compact solutions [1–3].

The work on the SPIC switch presented in this paper has been brought about by the needs of a new generation of power supplies. A schematic connection of the SPIC is shown in Fig. 1. A 700 V power MOSFET, oscillator, current limit and thermal shutdown circuit, and so on, are integrated onto a monolithic device.

The lateral double-diffusion MOS (LDMOS) transistor is considered as the device of choice when a high voltage power device is integrated monolithically with low voltage Bipolar-CMOS devices for SPIC. The Reduced SURface Field (RESURF) technique is the most widely used method for designing high breakdown voltage, low specific on resistance MOS device. However, the device reported herein is a novel double RESURF LDMOS fabricated using the optimum P-type multiple rings realized by implantation of impurity dopants through a mask having a sequence of opening and subsequent annealing. The widths and spacing between rings are optimized to achieve high voltage and the N-well drift region and the P-type multiple rings need to be fully depleted to achieve double RESURF theory [4–8].

SPIC's designing is always a difficult challenge. SPICs, especially those for high voltage operating environment, high voltage and large current are often encountered. The protecting circuits are, therefore, of importance. Some structures are proposed to sense the power MOSFET current or voltage, but these embodiments will make up a substantial total area and/or bring a trouble in layout [1,9–11]. In this paper, a versatile JFET device is firstly developed. The JFET device cannot only be used as the current detector, but also be used as the internal power supply for SPIC. Furthermore, the layout of the SPIC can be realized in one metal layer. When power MOSFET is in off state, the JFET device provides a convenient power source for control circuit and the like, eliminating the need for a bias winding and associated circuit. Despite the voltage of up to 700 V at the drain, JFET conduction channels pinch-off and keep the voltage at JFET tap from exceeding approximately 10 to 100 V. When the power MOSFET is in the on state, the JFET device can be used to sense the drain current. This connecting is therefore useful in the application where current limiting or similar functions are important.

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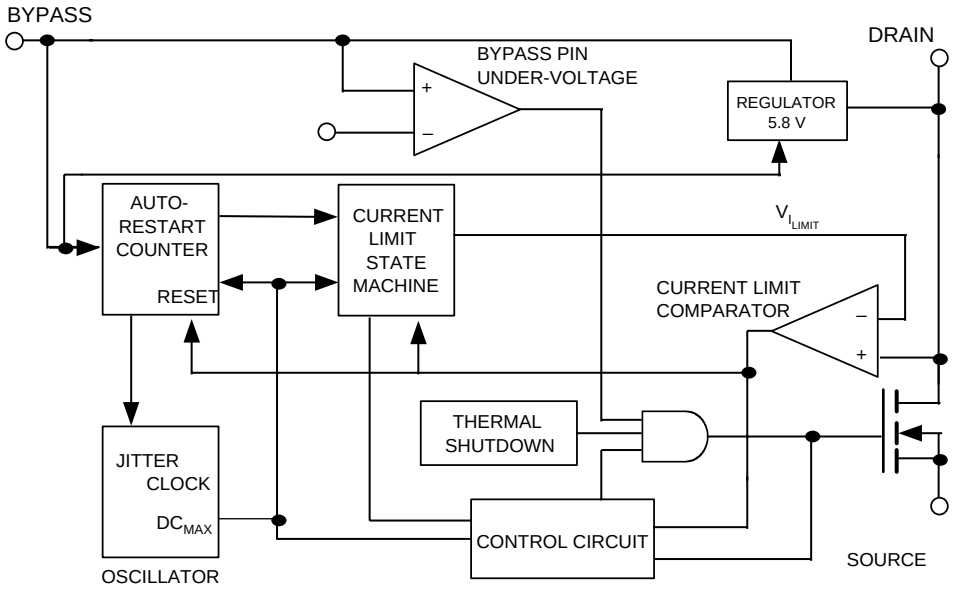

Fig. 1. A schematic connection of SPIC.

2. 700 V LDMOS structure

The proposed LDMOS structure shown in Fig. 2 is realized using a modified Bipolar-CMOS process in TSUPREM4 [12] and then imported into MEDICI [13] for device simulations. In this structure, the P-type multiple rings are inserted in the top of the N-well drift region. The widths and spacings between the rings are varied resulting in a lower drift region doping concentration near the source and a higher doping concentration near the drain to optimize the trade-off between the specific on resistance and the breakdown voltage. In addition, the double field plates are used in drain and source terminal to reduce the electric field peak and enhance the breakdown voltage.

The desired trade-off between breakdown voltage and the specific on resistance is obtained by varying drift region charge and P-type rings for the process used. Fig. 3 shows that the device breakdown voltage (BV) is highly dependent on the N-well dose in the drift region and it has a clear optimum.

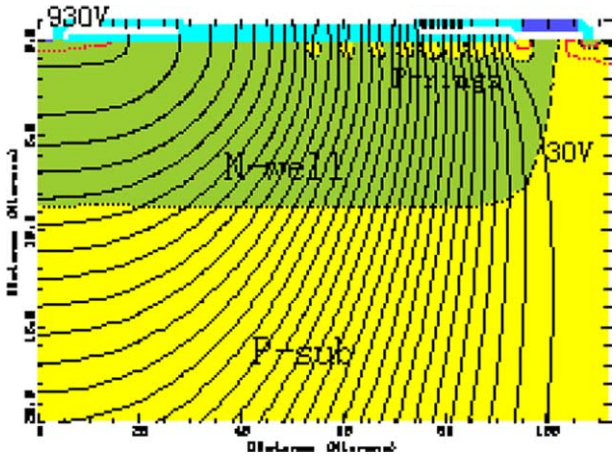

Fig. 2. The structure of the proposed double RESURF LDMOS and simulated potential contours at breakdown with optimum drift region dose.

The specific on resistance is decreased with increasing the N-well dose. Breakdown voltage as function of P-type rings dose for different N-well dose are shown in Fig. 4. As can be seen, for a fixed N-well dose, P-type dose has an optimum,

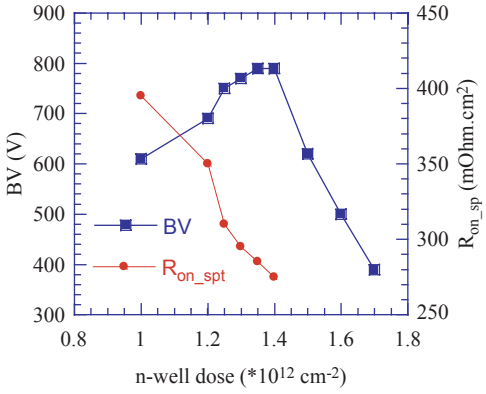

Fig. 3. Simulation the breakdown and specific on resistance as function of the N-well dose.

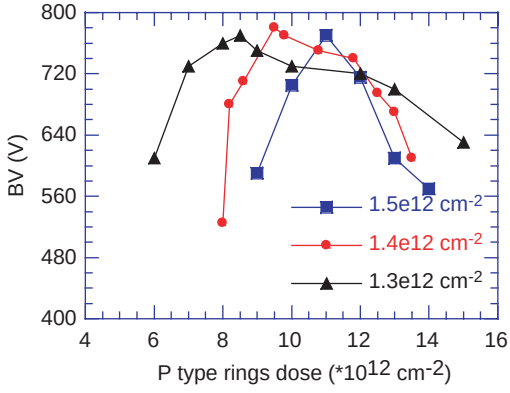

Fig. 4. Simulation the breakdown for different N-well dose as function of the P-top dose.