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# Effect of $RuO_2$ electrode on laser-MBE prepared $HfO_2$ gate dielectrics

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**Abstract**

In this paper, we report our recent study of the effect of $RuO_2$ as an alternative top electrode for pMOS devices to overcome the serious problems of polysilicon (poly-Si) gate depletion, high gate resistance and dopant penetration in the trend of down to 50 nm devices and beyond. The conductive oxide $RuO_2$, prepared by RF sputtering, was investigated as the gate electrode on the Laser MBE (LMBE) fabricated $HfO_2$ for pMOS devices. Structural, dielectric and electric properties were investigated. $RuO_2/HfO_2$/n-Si capacitors showed negligible flatband voltage shift (<10 mV), very strong breakdown strength (>10 MV $cm^{-1}$). Compared to the $SiO_2$ dielectric with the same EOT value, $RuO_2/HfO_2$/n-Si capacitors exhibited at least 4 orders of leakage current density reduction. The work function value of the $RuO_2$ top electrode was calculated to be about 5.0 eV by two methods, and the effective fixed oxide charge density was determined to be $3.3 \times 10^{12}$ $cm^{-2}$. All the results above indicate that $RuO_2$ is a promising alternative gate electrode for LMBE grown $HfO_2$ gate dielectrics.


*Keywords:* Metal gate; $RuO_2$; $HfO_2$; Gate dielectrics; Laser molecular beam epitaxy

## 1. Introduction

The scaling down of MOSFET device dimensions leads to the shrinking of the $SiO_2$ thickness [1]. When the quick-down thickness of $SiO_2$ is nearly approaching its physical limit of 3–4 atomic layers, the use of such ultrathin $SiO_2$ gate dielectric layer would result in many challenging issues, such as the high gate leakage current density, reduced drive current density, easy boron penetration into the gate and channel, serious reliability degradation, etc. [2]. To answer these critical technology challenges, in recent years, many high-*k* gate dielectrics have been extensively exploited and investigated to find potential replacements for $SiO_2$. Among many searched high-*k* dielectric material systems, $HfO_2$, with the dielectric constant in the range of 25–30, is the leading candidate and has been intensively studied [2–5]. One of the important considerations to choose $HfO_2$ as the high-*k* gate dielectric is its big energy bandgap of about 5.68 eV, which is generally larger than many other high-*k* candidates [5]. However, when the transistor gate channel length is scaled down below 50 nm, the depletion of poly-Si will become a very significant problem due to the active dopant density saturation [1,6]. Hence, alternative gate electrodes should be employed to replace the poly-Si gate in future MOSFET device with dimension of 50 nm or below [7–9].

According to the ITRS roadmap, electrode materials with high work function (~5 eV) such as Pt, Ru, Ni and $RuO_2$ are promising candidates for pMOS transistors [1]. $RuO_2$, especially, has many additional desirable properties such as good integration with high-*k* dielectrics, good etching properties, excellent thermal stability, and inhabitation to the oxygen diffusion [10–14]. Therefore, in this paper, we report our results and analysis on structural property of $RuO_2$ layer, and the electrical properties of $RuO_2/HfO_2$ gate stack. The $HfO_2$ thin films were deposited by LMBE system.

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## 2. Experimental details

### 2.1. Device fabrication

$HfO_2$ films were deposited onto (1 0 0) oriented n-type silicon wafers with 1–10 Ω cm resistivity by the KrF excimer LMBE technique which was described in detail elsewhere [15]. The RCA cleaned wafers were immediately loaded into the LMBE deposition chamber. The $HfO_2$ films were deposited by the ablation from a hafnium target in $O_2$ ambient with the substrate temperature held at 500 °C. The power density of the laser beam was fixed at 1.8 J $cm^{-2}$ and the laser pulse repetition rate was 2 Hz. The deposition pressure was $2 \times 10^{-4}$ Torr. Post deposition annealing (PDA) was performed ex situ in a rapid thermal annealing (RTA) chamber at 500 °C for 30 s in $N_2$ ambient. For the $RuO_2/HfO_2/Si$ stack, Ru metal was used as the target and $RuO_2$ top electrode was deposited in $O_2$ ambient at room temperature using an RF magnetron sputtering system. The films were patterned using the lift-off lithography with an active area of $1 \times 10^{-4}$ $cm^2$. Finally, the backside of the wafer was etched and deposited with aluminum to form an ohmic contact.

The microstructure of the $RuO_2$ films was characterized by a Siemens D5005 X-ray diffractometer with grazing angle of 2°. An HP4284A Precision LCR meter was used to perform the *C–V* measurement in various frequencies. An HP4155B semiconductor parameter analyzer was used to measure the *I–V* behavior.

### 2.2. Work function extraction methodology

Two methods are described here in order to calculate the work function of the $RuO_2$ gate electrode.

In the first method, under the assumption that the fixed oxide charge in the dielectric $qN_{\text{eff}}$ is mainly located at the $HfO_2$–Si interface, which means the effective charge density $N_{\text{eff}}$ is independent of the dielectric thickness, the work function $\phi_m$ can be described by as below [17]

$$\phi_m = \phi_{Si} + V_{FB} + \frac{qN_{\text{eff}}}{\varepsilon_{ox}} t_{ox}, \quad (1)$$

where $\phi_{Si}$ is the work function of the Si substrate, $t_{ox}$ is the oxide thickness and $q$ is the electric charge. Under the above assumption, $V_{FB}$ is measured as a function of $t_{ox}$. A straight line plot of $V_{FB}$ versus $t_{ox}$ yields a slope equal to $qN_{\text{eff}}/\varepsilon_{ox}$, and then $N_{\text{eff}}$ can be derived. Meanwhile, since $\phi_{Si}$ is known, the value of $\phi_m$ can also be obtained at the interception for $t = 0$. This method is generally used in the extraction of the work function [10,11,17].

In addition, the work function value of $\phi_m$ can also be obtained by comparing the flatband voltage shifts of MOS capacitors made using different gate electrodes [16]. To obtain the $\phi_{RuO_2}$, the value of $\phi_m$ for another metal electrode should be known independently from a photoemission measurement for the reference and comparison purpose. From the high frequency *C–V* curves taken using the reference and $RuO_2$ gate metals, the difference in flatband voltage can be directly determined. In addition, the terms in Eq. (1) due to $qN_{\text{eff}}$ can be cancelled out because $qN_{\text{eff}}$ is the same for the two capacitors, then Eq. (1) can be rewritten as

$$(V_{FB})_{\text{reference}} - (V_{FB})_{RuO_2} = \phi_{\text{referencet}} - \phi_{RuO_2}. \quad (2)$$

If $\phi_{\text{referencet}}$ is known, $\phi_{RuO_2}$ can then be calculated. Unlike the first method, this method is seldom used in the extraction of metal work function. In our work, we also employ this method to verify the validity of the work function result extracted from the first method.

## 3. Results and discussion

### 3.1. XRD observation

The XRD pattern of the sputtered $RuO_2$ film is shown in Fig. 1. It is clearly seen from this figure that even though the film was deposited at room temperature, the $RuO_2$ is in the polycrystalline phase and the diffraction peaks match the stoichiometric $RuO_2$ crystal phase [10].

### 3.2. Capacitance–voltage (C–V) characteristics

The *C–V* measurement of $RuO_2/HfO_2/Si$ gate stack at various frequencies is depicted in Fig. 2. As seen from the figure, when $V_g < -0.75$ V, the MOS capacitor in depletion shows almost no dependence on the frequency. However, with the $V_g$ further increased from −0.75 to 0.3 V, the capacitor, changed from inversion to accumulation, exhibits some capacitance dispersion which may be caused by the presence of the leakage current and the too large series resistance as discussed by Norton [16]. In such a case, the low frequency data is not quite reliable, and therefore the capacitance measured at 1 MHz is used to calculate the more accurate equivalent oxide thickness (EOT).

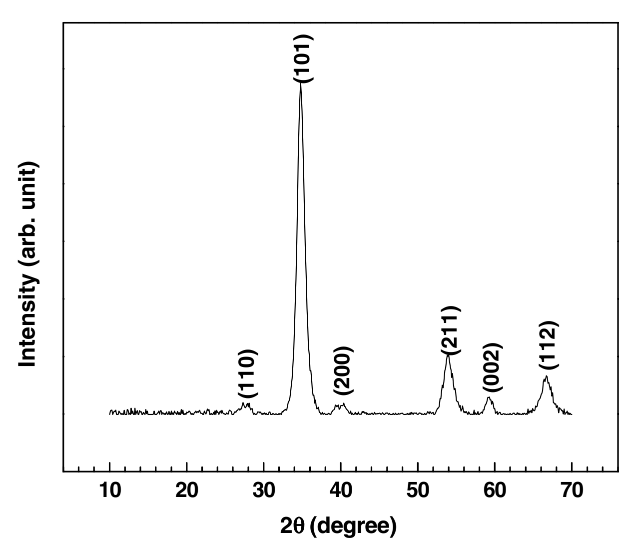


Fig. 1. X-ray diffraction of the sputtered $RuO_2$ film.