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Representation of strained gate-all-around junctionless tunneling nanowire filed effect transistor for analog applications

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ABSTRACT

In this paper, we investigated gate-all-around silicon nanowire (NW)-based junctionless tunnel field effect transistor (FET) which is called junctionless tunnel NWFET (JL-TNWFET) with the impact of variation of amount of uniaxial tensile strain on band-to-band tunneling (BTBT) injection and electrical characteristics. The tunneling model is first calculated for measurements of gate-controlled BTBT in the JL-TNWFET and is compared with the strained JL-TNWFET with similar technology parameters. The simulation results show that the JL-TNWFET have potential for low-operating-voltage application (V_{dd} $_amp_$lt; 0.4 V) and represent high I_{ON}/I_{OFF} ratio and steep subthreshold swing over many decade while encompassing high *ON*-state currents. Whereas, the strained JL-TNWFET due to thinner tunneling barrier at the source-channel junction which leads to the increase of carrier tunneling rate shows excellent characteristics with high ON-current, superior transconductance (g_m) and cut-off frequency (f_T).

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1. Introduction

In recent years, some novel devices based on different mechanisms have been reported in response to the limit of the traditional MOSFET scaling. The tunneling field effect transistors (TFETs) is one of the alternative devices to replace CMOS technology, which is most suitable for low-power applications [1]. Because such devices utilize tunneling injection of carriers through a tunneling barrier rather than thermionic injection over a barrier, and the barrier width can be controlled by the gate voltage, they have good immunity to short channel effect, drain induced barrier lowering, and superior electrostatic control (lower OFF-current and steeper subthreshold swing) which enabling transistor operation at voltage below 0.5 V [2,3]. However, quantum mechanical tunneling in these devices is insufficient due to the relatively large band gap (1.1 eV), indirect energy gap of Si, and therefore the ON-current in such transistors is limited. For achieving higher tunneling currents, semiconductors with lower band gap Eg are required [4,5]. III-V materials with direct band gap offer distinguished advantages in achieving high tunneling currents [6,7]. However, their adaptability with Si processing and the poor high-k interface are still the main limitations for III-V tunnel FETs. Also, Strain engineering technologies to enhance MOSFETs mobility have been extensively investigated [8] and already widely used in mass production. Moreover, it has been shown that tensile strained Si significantly improves tunneling currents [9, 10]. This advancement stems from the effect, that uniaxial strain in Si nanowires along the [110]-direction picks up the subband degeneracy of the valence and conduction bands, leading to reduction of the effective mass m* of electrons and holes [11]. Furthermore, SiGe is an attractive material for make utilizing in TFETs because of its lower Eg [12,13]. However, recently a new structure named junctionless tunnel field effect transistor (JLTFET) has been proposed which is tunnel FET without any abrupt doping profile [14,15,27]. It has presented good ON-state current and low subthreshold swing as blends advantages of JLFETs and TFETs. JLTFET also feature lower subthreshold slope than conventional MOSFET and JLFET at the room temperature opens new future for low power application devices [16]. In this paper, we have examined a gate-all-around junctionless tunneling nanowire-based FET (JL-TNWFET) structure with and without uniaxial tensile strain, in order to achieve superiority of all three the JLFET, the conventional TFET and uniaxial tensile strain incorporated together. Then, we present the simulation results exhibiting considerably enhanced gate-controlled band-to-band tunneling (BTBT) current and radio frequency (RF) metrics due to using highly uniaxial tensile strained Si ($E_g = 0.865$ eV) in the JL-TNWFET.

2. Device structure and simulation

Fig. 1 shows a schematic of the gate-all-around junctionless tunneling nanowire field effect transistor (JL-TNWFET) structure in conjunction with the lengths and thickness of layers, which used in simulation. The simulated device is fundamentally a junctionless transistor uses n^+-doped strained silicon along the [100]-direction with uniform doping concentration of (1×10^{19} cm^{-3}) which placed throughout the source, drain and channel regions. The proposed JL-

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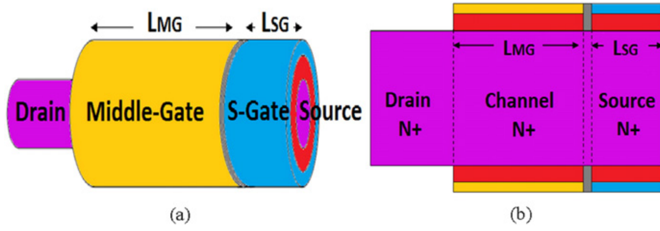

Fig. 1. (a) Sketch of the gate-all-around JL-TNWFET (b) and its cross section along z-axis. For the gate-all-around JL-TNWFET, the gate near the tunneling region is named as middle-gate (MG), and the other is denoted as side-gate (SG).

TNWFET utilizes two isolated gates (Middle-Gate, Side-Gate) with two work functions to treat like a tunnel field effect transistor (TFET). The length of the channel is 40 nm and the length of the source and drain regions is 30 nm. The radius of the strained nanowire (T_{si}) is on the order of 5 nm, oxide thickness (T_{ox}) is 2 nm and the isolation layer in between middle-gate (MG) and side-gate (SG) electrode is 2 nm which works as spacer between the gates. The gate-all-around structure is used to provide better electrostatic controllability of gate over channel. Preset parameters used for device simulation of JL-TNWFET as in Fig. 1 are tabulated in Table 1.

In order to make the layers beneath middle-gate (MG) and side-gate (SG) intrinsic and *p*-type, respectively, we have chosen 4.38 eV and 5.92 eV for the MG and SG electrode, to increasing electrons populations below the gate and give the superior result in terms of ON/OFF-state current values for the both devices. The integration of MG and SG together in the fabrication process, whose workfunctions are different, could be done by using the techniques as reported in Refs. [17–19]. The formation of the isolation layer with thickness of 2 nm of SiO2 could be done either by using a sputtering process or by a modern photolithography process (such as electron beam lithography, X-ray lithography, extreme ultraviolet lithography, and ion projection lithography) after formation of the field oxide by wet oxidation.

The key parameter of the investigated device is the constant uniaxial tensile strain which has an equal level along the device direction. The high level of uniaxial tensile strain along the device induces a local band gap constriction. The band gap (E_g) corresponding non-strained Si JL-TNWFET is assumed to be 1.1 eV, similar to bulk Si. Depending on the earlier reported works in [20,21], 0.2 eV band gap constriction in Si can correspond to 3 or 5 GPa uniaxial tensile stress, respectively. Both expected amounts of stress are below the yield strength of Si (7 GPa for bulk Si [22]) and therefore, $_amp_$gt; 0.2 eV local constriction of band gap can be accessible by local strain engineering. In this way, we have assumed the band diagram profile along the channel for reference JL-TNWFET with band gap (E_g) = 1.1 eV and also, for highly constant strain profile channel with band gap (E_g) = 0.865 eV. Fig. 2 presents the (a) OFF-state, and (b) ON-state of the simulated energy band diagrams of the device that illustrate the basic operation of JL-TNWFET versus strained JL-TNWFET. In the absence of gate voltage, the tunneling barrier width in between source and channel junction in the case of JL-TNWFET is large enough to give extremely small current

Table 1
Preset Parameters for device simulation of JL-TNWFET.

Parameter	Value
Source/drain/channel doping (N_D)	1×10^{19} cm^{-3}
Effective oxide thickness (T_{ox})	2 nm
Middle-gate workfunction (Φ_{MG})	4.38 eV
Side-gate workfunction (Φ_{SG})	5.92 eV
Gate length (L_g)	40 nm
Source/drain length ($L_{s,d}$)	30 nm
Channel thickness (Tsi)	10 nm
Supply voltage (V_{DD})	1 V
Permittivity of gate dielectric material (εd)	3.9

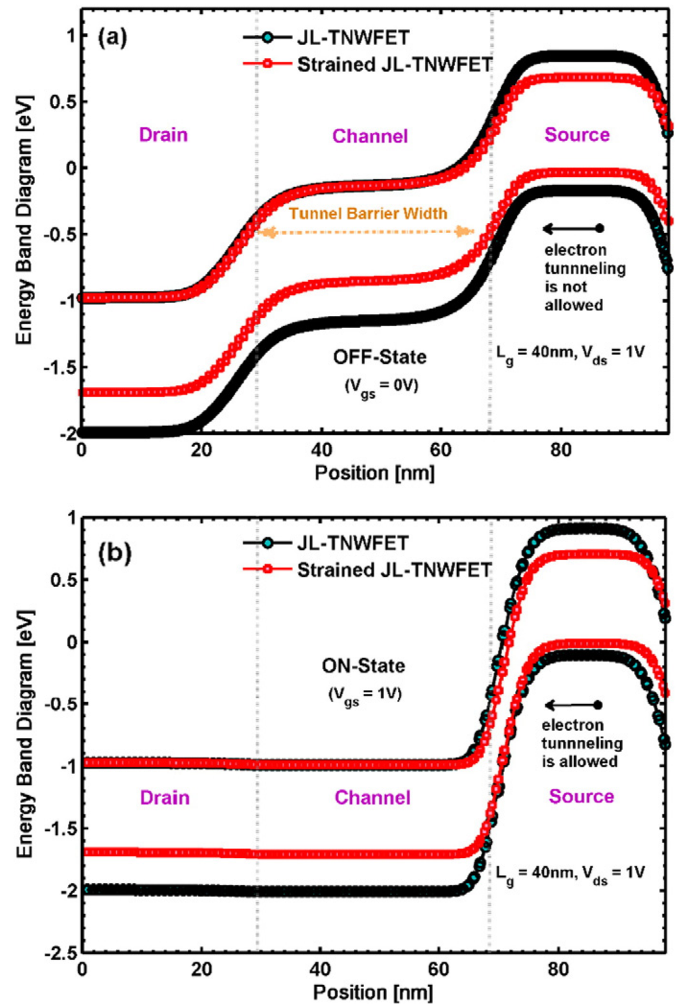

Fig. 2. (a) OFF-state ($V_D = 1$ V, $V_{MG} = 0$ V) and (b) ON-state ($V_D = 1$ V, $V_{MG} = 1$ V) energy band diagrams of JL-TNWFET and strained JL-TNWFET.

(I_{OFF}) and the probability of band-to-band tunneling of electrons is negligible. However, in the strained JL-TNWFET, as expected, the tunneling barrier between source and channel reduced as we apply uniaxial tensile strain. This feature of shortening the OFF-state tunneling barrier has key function in increase of BTBT current, as well as increasing the transition probability of the carriers. As the gate voltage become increasingly positive from the OFF-state, both of JL-TNWFET and strained JL-TNWFET bands at the source-end will bend more and making the tunneling barrier increasingly thinner. Accordingly, the strained device formed the narrower tunneling barrier at the source-channel interface for conducting a high ON-state tunneling current. The OFF-state (a) and ON-state (b) of the electric field profile of the JL-TNWFET against strained JL-TNWFET are shown in Fig. 3. In the OFF-state, for both structures due to the formation of band diagram looks like N^+-I-P^+ doped device structure, it has been created two electric field peaks at the source-channel and drain-channel junction. Simultaneously, the strained JL-TNWFET because of smaller tunneling barrier has lower values of lateral electric field which leads to the increase of carrier tunneling. However, in the ON-state, due to the presence of gate-to-source voltage, the band diagram profile behave similar to N^+-N-P^+ doped device structure, so it has been created one strong electric filed peak at the source-channel junction which implicates the tunneling probability goes up in that region and the reason of this superiority is the further quantum tunneling phenomenon. Although, the strained JL-NWFET has performance enhancement because of the application

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