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Monolithic 3D TSV-based high-voltage, high-temperature capacitors

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ABSTRACT

In this work, high-voltage monolithic 3D capacitors operating at 100 V (6 MV/cm) are fabricated by the use of a through silicon-via-based technology. Electric characteristics of the monolithic 3D capacitors exhibit a capacitance density of 17 times larger than that of the planar capacitors with an equal contact area and identical dielectric thicknesses. The impact of the 3D architecture of capacitors on their electrical properties is studied for various patterns and geometries. TSV-based capacitors with a hexagonal arrangement of the holes and 20 μm hole diameters exhibit a capacitance deviation of 0.8% at 150 °C in accumulation, justifying the capability of TSV-based capacitors to operate even at high-temperatures. Furthermore, a high dielectric-breakdown voltage of 280 V (18 MV/cm) was realized using a thick hybrid dielectric stack of SiO_2/Si_3N_4.

1. Introduction

The integration of capacitors into silicon planar technology is an attractive field of study due to its suitability in numerous applications. Monolithic 3D capacitors show outstanding features such as a high-integration-density and the capability of operating at high-voltages in a wide range of temperatures [1,2]. These monolithic capacitors are utilizing the third dimension to enlarge the capacitor area significantly without any increase in the capacitor footprint.

The enlarged Si-surface was proposed for the first time by Bean [3], and was developed into the ultra-deep trenches by Lehmann [4]. The CMOS-compatible fabrication process for the integration of the C-link capacitors is based on a conventional through-silicon-via (TSV) technology by transferring the design of the hole-patterns through photolithography onto the Si-substrate. The integrated capacitors in Si-substrates utilizing TSV-based technology have become promising candidates to replace with conventional bulky and expensive capacitors [5–8]. In addition, beyond the capability of covering a wide temperature range and flexibility in the application, these integrated capacitors have to withstand the high voltages for specific applications.

In the present work, we report on the fabrication technology as well as the electrical characterization of monolithic 3D capacitors desired for operating at 100 V for applications in monolithic integrated DC–DC converters. In order to accomplish the desired operating voltage, a thick hybrid dielectric stack consisting of SiO_2 ($\varepsilon_r = 3.9$) and Si_3N_4 ($\varepsilon_r = 7.5$) [9] is applied. Although there are many efforts to improve capacitance density in thin-film capacitors using high-k dielectric materials such as $BaTiO_3$ ($\varepsilon_r = 220$) and PZT ($\varepsilon_r = 1000$) [10], still the integrated capacitors based on the traditional SiO_2 and Si_3N_4 demonstrate higher integration density, high breakdown voltage, and less sensitivity to the temperature deviation during packaging and operation, which is not the case in most of high-k materials [1,10,11].

The formation of metal electrodes in the area of atomic layer deposition (ALD) followed by wet-etching techniques has been known as an excellent step coverage of the deposited layers [12]. However, the advantage here is the simplicity of the metallization, in which no further metal-etching step is demanded after metal layer deposition.

In the following, the manufacturing process and technology are explained. Electrical characteristics of the 3D capacitors based on the different geometry structures of hole-patterns are shown and compared with those of planar-capacitors. The results demonstrate the applicability of using TSV technology to implement high-density and high-voltage capacitors in integrated circuits such as in smart-power ICs.

2. Materials and methods

Boron-doped silicon wafers of 150 mm diameter with resistivity of 0.01 Ωcm were utilized as substrates. An illustration of the device fabrication process is shown schematically in Fig. 1.

On equal terms of the TSV-structures' formation, the Si-substrate was patterned using the advanced silicon etch (ASE) process [13]. For this purpose, a thin oxide layer was thermally grown onto the Si-substrate and used as a hard mask (Fig. 1a). Circle-patterns were transferred onto the surface applying photolithography (Fig. 1b). Patterns of the circles with diameters of 20 and 40 μm, and 5–15 μm pitch between circles were formed onto the Si-substrate. Both hexagonal and orthogonal layouts shown in Fig. 2 were applied for the hole-pattern arrangements.

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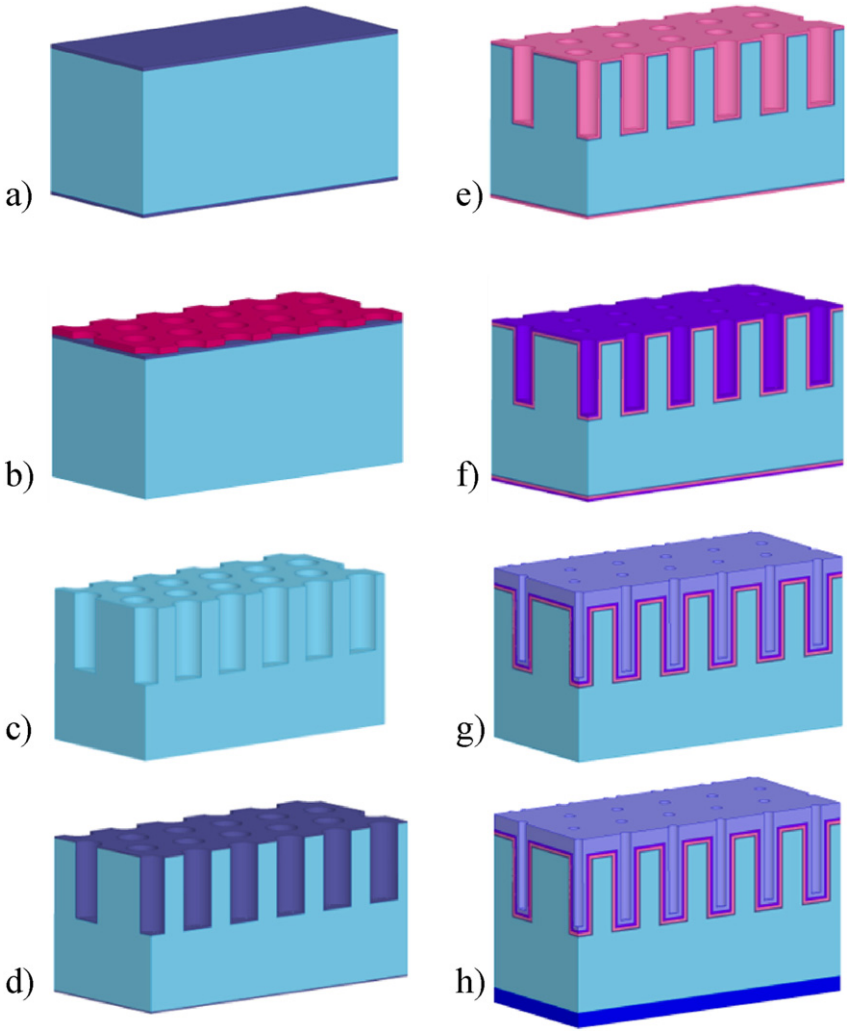

Fig. 1. Schematic view of the simplified fabrication process for TSV-based capacitors. a) thermal growth of oxide as a hard mask on Si- substrate, b) first photolithography transferring design of holes onto the surface, developing the photoresist, c) dry etching of Si, removing photoresist, growth and removal sacrificial oxide layer, d) thermal growth of the first dielectric layer SiO_2, e) LPCVD of the second dielectric layer Si_3N_4, f) LPCVD of poly-Si, g) patterning the top electrode, h) processing bottom electrode by sputtering Al and evaporation of Cr/Ni/Ag.

After patterning the resist and oxide layers, the Si-substrate was etched with an ASE process (Fig. 1c). To obtain the straight structures free of voids in the ASE process, the etching time and passivation ratio were optimized. Next, a thin SiO_2 layer with thickness of 20 nm was grown on the surface by dry oxidation.

This sacrificial oxide layer was used for cleaning the surface as well as for repairing the crystal defects formed by the reactive ion etching process inside the hole-patterns. The sacrificial oxide layer was removed afterwards. For the hybrid dielectric layer, a 20 nm-thick SiO_2 layer was grown by dry oxidation followed by a low-pressure chemical vapor deposition (LPCVD) of Si_3N_4 with nominal thickness of 280 nm (Fig. 1d and e).

Fabrication of the top electrode was realized by in-situ doped poly-Si with thickness of 500 nm deposited via LPCVD (Fig. 1f). The

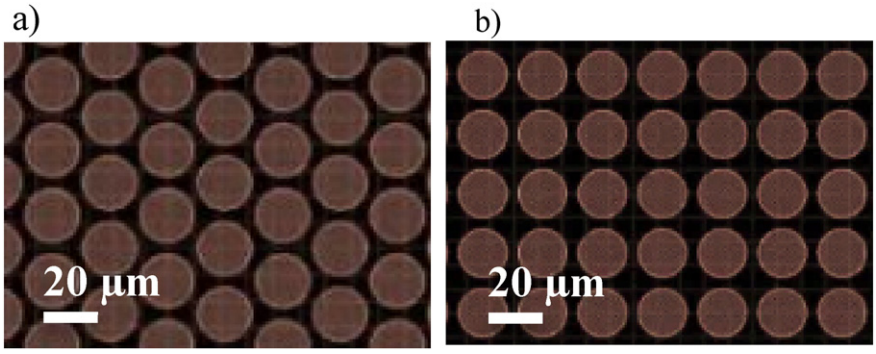

Fig. 2. Layout variations with a) hexagonal and b) orthogonal arrangements.