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Stress analysis of airgaps under process-induced thermo-mechanical loads

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ABSTRACT

In order to understand the state of process induced stresses in airgap interconnect structures fabricated by the etch-back approach, finite element (FE) models of a 90 nm pitch interconnect were developed and a stress analysis of the structure was conducted as a function of the dielectric liner (silicon nitride) and metal barrier (MB) thicknesses. Models of similar structures without airgaps were also developed and the stresses were evaluated as a benchmark case. In addition, a static field solver was used to extract the capacitance of the interconnect structure and evaluate the capacitance reduction by introducing airgaps compared to structures without airgaps. The results identified the sidewall dielectric liner as a critical location where high tensile stress concentration can result in failure of structures under thermo-mechanical loads. Reducing the thickness of the MB and the dielectric liner simultaneously to 1 nm and 2 nm respectively, minimized metal barrier tensile stresses but increased the tensile stress in the dielectric liner dramatically to 1 GPa. Meanwhile, this configuration provided the lowest capacitance and reduced the capacitance of the interconnect by 27% compared to a similar structure without airgaps. In general, reducing the thickness of the MB decreased its stresses both in interconnect structures with and without airgaps.

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1. Introduction

The performance of ultra large scale integration (ULSI) integrated circuits is limited by the resistive and capacitive (RC) delays in the interconnect [1]. This challenge necessitates development of technologies that reduce resistances and capacitances. Moreover, interconnect capacitance also entails excessive interconnect cross-talk and power dissipation that underlines the importance of capacitance mitigation. Therefore, novel inter-line ultra-low-k dielectric materials (ULK) with k values lower than 2.5 have been employed whereby the k value is further reduced by inclusion of pores into the dielectric material to form porous low-k materials [2].

Nonetheless, as the porosity of the ULK materials is increased, their mechanical properties deteriorate dramatically which constitutes a major integration challenge [3]. ULK materials suffer from lower stiffness, low fracture toughness and inferior adhesion mainly due to their porous structure which renders them susceptible to damage during the Damascene process steps [3,4]. This dramatic reduction of mechanical robustness of ULK materials constitutes a limit for further lowering the effective k value. Therefore, although integration of ULK materials has led to a considerable reduction of interconnect capacitive delay, currently there is a significant effort ongoing for replacing the interline dielectric fully with air by integration of airgaps given that air offers the best dielectric constant value of 1 [5–9]. However, implementing airgaps adds further to the integration challenge which necessitates a thorough understanding of the stress state of the interconnect structure and the impact of each process step [10].

One of the potential airgap integration approaches is the etch-back approach where the inter-line low-k is removed by an etch step [10]. However, in order to ensure mechanical stability and chemical stability of such a structure, it is necessary to implement a relatively stiff dielectric liner such as silicon nitride to cover the metal structure which prevents oxidation of the metal and also provides mechanical support and stability to the airgap and metal lines [10,11]. Process induced stresses not only can complicate interconnect integration itself, but also will have important implications for reliability under chip package interaction (CPI) and electro-migration (EM) loads. Tensile hydrostatic stresses in copper lines facilitate EM induced void formation [12] and also expansion of copper due to thermal effects or EM induced extrusion can lead to airgap failure at the liner or MB. Specifically, as the inter-line space is down-scaled it is necessary to reduce the thickness of the liner to ensure capacitance reduction and that can potentially constitute a reliability challenge as the stiff liner will be compromised [11]. Clearly therefore, it is of outmost importance to devise methodologies that provide quantitative understanding of the process induced interconnect stresses. To this end, in this study numerical models of interconnect structures are developed in order to investigate the mechanical stresses and shed light on the influence of two main airgap design parameters for the etch-back approach, (i) the thickness of the metal barrier (MB)

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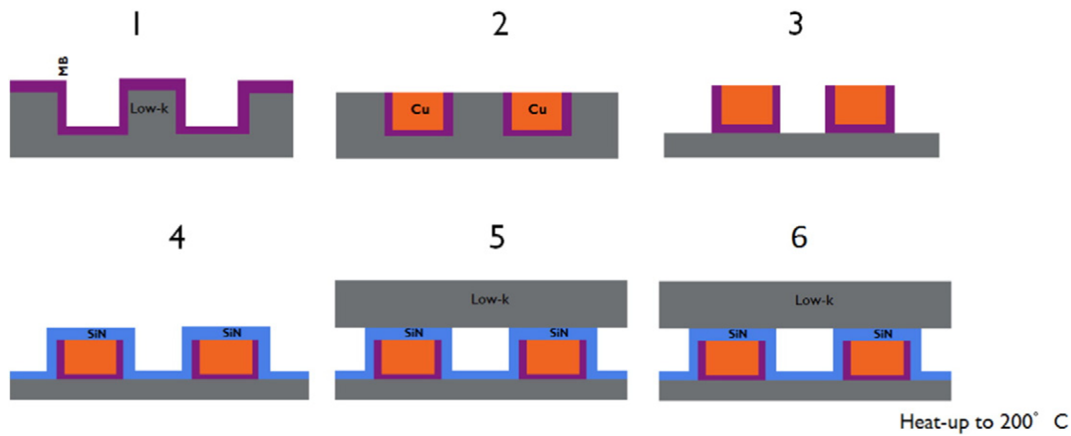

Fig. 1. Summary of the modeled process steps.

and (ii) the thickness of the dielectric liner and also to devise potential strategies for stress mitigation.

2. Methods

2.1. Stress analysis

A 2D plane strain FE model of a single level interconnect structure with 90 nm pitch and line aspect ratio of 1 was developed within the MSC-Marc® FEM package. Two groups of interconnect structures were modeled; (i) the mainstream structure with ULK without airgaps and (ii) similar structures but with airgaps using the etch-back process. In order to model the deposition of each material, elements corresponding to each material were activated at each subsequent analysis step of the multistep thermo-mechanical simulation, see Fig. 1. The model was discretized using solid planar quadrilateral plane-strain elements (element type 11 in MSC-Marc® FEM package) and approximately 800–1000 elements were used to model each line structure. The existing stresses within each deposited material, in addition to the thermal expansion mismatch, are induced due to complex molecular/atomic re-organization during deposition. In order to capture the overall effect of such phenomena, the intrinsic stress of each material was extracted from the wafer bowing experiments on single blanket layers using the Stoney's approach (Table 1) [13]. Subsequently, the intrinsic stress values were implemented in the FE model by including stress initial conditions in each step of the simulation which were allowed to reach an equilibrium state during the step. Airgap formation in the etch-back process was modeled by deactivation of intermetallic ULK related FE elements. Ultimately a heat-up step of 200 °C was applied to the sequentially built-up structure in order to investigate the stresses at elevated temperatures, specifically the ability of the airgaps to withstand copper expansion without failure. The mechanical and thermal material properties used in the simulations are summarized in Table 2. In order to understand the variation in stresses of copper lines, MB and the dielectric liner with the thickness, the thickness of the MB was altered from 1 to 6 nm and the thickness of the dielectric liner from 2 to 10 nm at the sidewall whilst it was presumed that the thickness of the liner at the top of the liner is twice the thickness of the liner at the sidewall i.e. (4–20 nm). The copper line dimensions were kept constant. Interconnect mechanical failures are mainly brittle cracking events specifically given the low fracture toughness and adhesion of the low-k dielectrics and the dramatic dimensional downscaling of copper lines [4,14,15]. Such brittle mechanical failures have been shown to be driven by the maximum tensile principal stresses [14–16]. Therefore, in this paper the maximum principal stresses are reported for the dielectric liner and MB. On the other hand, the hydrostatic stresses in copper are also reported given that hydrostatic stress is a predictor of electro-migration and stress migration [16,17].

Table 1
Intrinsic stresses obtained from wafer bowing.

Layer	Thickness (nm)	Residual Stress (MPa)
Low-k (OSG 2.4)	100	+40 (tensile)
MB (Ta)	7	−1375 (compressive)
Liner (silicon nitride)	20	−120 (compressive)
Cu	60	+500 (tensile)

2.2. Capacitance analysis

Capacitance models of the interconnect structure were developed using the Raphael™ field solver [11,18] and the various designs were simulated consistent with the case studies discussed for the mechanical model by interfacing Raphael™ with the Optimus™ software. The capacitance of the airgapped interconnects were benchmarked against a similar structure but with the mainstream technology (i.e. without airgaps and using ULK material with a k = 2.4) to decipher the capacitance benefits when incorporating airgaps. The capacitance value is the total capacitance including the capacitance of the line with the two neighboring lines and the top and bottom lines presuming a Manhattan interconnect structure. The dielectric barrier and liner material were considered to be silicon nitride with a dielectric constant of 7.3 and the k value of the ULK was set to 2.4 in all cases.

3. Results and discussion

The stresses in the interconnect structure were calculated using the developed FE model as a function of MB and dielectric liner thickness. The dielectric liner was found to endure highest tensile maximum principal stresses at the sidewall compared to MB, see Fig. 2. In the case were the thickest MB and dielectric liner were implemented (i.e. 6 nm MB and 10 nm liner) the maximum principal stresses reached 628 MPa in the liner and 255 MPa in MB. In contrast the thinnest MB and liner within the studied range resulted in a liner maximum principal stress of

Table 2
Thermal and mechanical material properties used in the simulations.

Material	Young's modulus (GPa)	Poisson's ratio	Coefficient of thermal expansion (CTE)
Low-k organo-silicate glass with k value of 2.4 (OSG 2.4)	9	0.2	1.2×10^{-5}
MB (Ta)	186	0.34	6.3×10^{-6}
Liner (silicon nitride)	265	0.27	1.5×10^{-6}
Cu	117	0.3	1.67×10^{-5}

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