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Single- and multilayer graphene wires as alternative interconnects

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ABSTRACT

In this work, we evaluate the material properties of graphene and assess the potential application of graphene to replace copper wires in Back-End-Of-Line (BEOL) interconnects. Based on circuit and system-level simulations, high restrictions are imposed to graphene with respect to contact resistance and mean free path. Experimentally we evaluate single and multi-layer graphene wires and we measure carrier mean free paths (MFPs) above ~110 nm. However, contact engineering will be the key issue for integration of graphene as interconnect.

1. Introduction

The continued scaling requirements for the future technology nodes, require a continuous search to meet the specifications. Apart from the traditional BEOL interconnects such as copper [1,2] and tungsten [3,4], we will evaluate the potential of graphene as a replacement for the currently used metals.

With the aggressive dimension scaling, traditional interconnects are expected to suffer from a reduced conductivity and a higher wire resistivity. In addition, crosstalk between the neighboring wires becomes important, as well as electromigration and thermally induced degradation [5]. Graphene is emerging as a competitive solution, because of its high current carrying capacity, high electrical and thermal conductivity and immunity to electromigration [6].

In a recently published paper by Pan et al. [7] a theoretical evaluation of graphene is reported based on realistic circuit- and system-level simulations. It is clear that the wire dimensions of graphene, both in length and width, have a major impact on the delay and the energy-delay product (EDP). The optimal delay improvement is obtained for the longer wires, however tight restrictions are imposed on the mean free path (MFP). Additionally, the number of graphene layers plays a crucial role. Independent of the wire length, multiple graphene layers are required to reach the optimal delay improvement. Depending on those MFP values (ranging between 0.1–1.2 μm), fewer layers are needed ranging from about ~15 up to even 60 layers. As the wire length increases, a higher number of layers are necessary to sustain a reasonable delay improvement. Upon improvement of MFP the variations are reduced. This opens the possibility of fine-tuning the graphene stacks in order to achieve the optimal performance.

In this work we have studied graphene contact resistance and mean free path experimentally and compared with the simulations. In the first part of the work the electrical properties of single-layer graphene wires are evaluated while their dimensions are scaled down to 40 nm. Subsequently, the performance of multilayer graphene stacks for interconnects is evaluated.

2. Materials and methods

We use the Transfer Length Method (TLM) [8] to extract simultaneously the contact resistance (Rc) and the sheet resistance (Rs). Metal contacts are placed on a graphene stripe with varying spacing L between the contacts. The measured total resistance (R_{tot}) is plotted as a function of the graphene channel length L, and from the linear fitting parameters, Rc is extracted from the intercept value, while the slope is representative for the Rs (Fig. 1d–e).

Currently various sources of graphene are available [9]. Graphene flakes (single- or multilayer) are exfoliated from highly oriented pyrolytic graphite (HOPG). Micromechanical exfoliation of HOPG, also referred to as the “scotch-tape method”, was used originally for the

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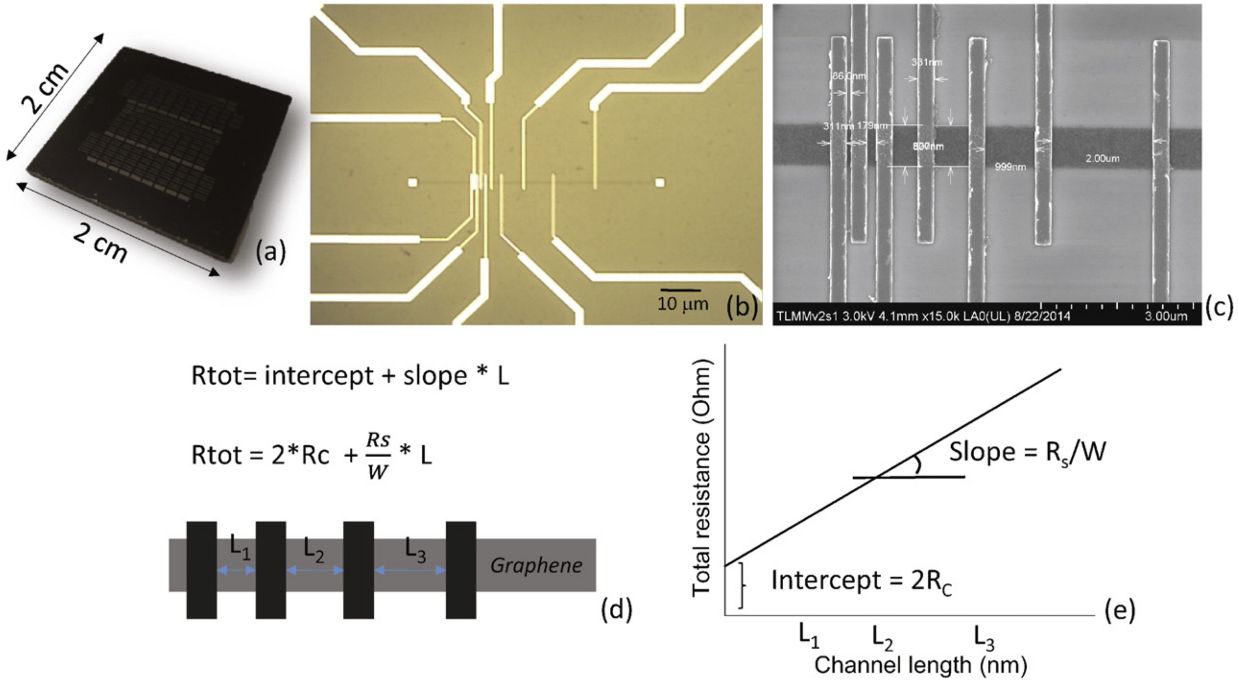

Fig. 1. Image (a) of large area graphene processed with a broad set of test structures allowing for statistical analysis. (b) Optical microscope and (c) SEM image zoom-in on a processed TLM structure confirming the designed dimensions. (d) Schematic representation of the device layout and (e) linear fitting equation.

isolation and electrical study of graphene for the first time [10]. Although this is a high quality material and thus the principal choice for fundamental graphene research, it is not suitable for large area industrial applications. Regarding large-area synthetic graphene the most commonly used growth process is chemical vapor deposition (CVD) catalyzed by metals, typically Cu [11]. Since these processes are done at elevated temperatures (above 650 °C), the obtained graphene needs to undergo a transfer step on a target substrate. Graphene of different quality (grain boundaries) and multilayer stacks can be obtained by fine tuning the process.

For this work, we use both CVD single-layer graphene (SLG) patterned in ribbons and exfoliated single- and multilayer graphene flakes (MLG). A systematic study is performed in order to evaluate the variation in contact resistance and mean free path as the wire dimensions are scaled and the layer thickness is increased.

CVD graphene was grown on a CuNi alloy at 750 °C [12]. Afterwards a PMMA-assisted transfer onto a Si/SiO_2 substrate was performed [13]. HOPG from "SPI Supplies" was purchased for the mechanical exfoliation of single- and multilayer graphene flakes. In Fig. 2 Raman plots of both CVD and exfoliated single-layer graphene are shown. The appearance of D-peak denotes the presence of defects in the carbon lattice. Also the ratio between the 2D/G peak is indicative of the quality of the layer. The sharpness of the 2D-peak is indicative of the number of graphene layers present [14]. For the CVD graphene used in this study $I_G/I_D \sim 1.9$ and $I_{2D}/I_G \sim 1.25$. We observe the absence of D-peak and a higher ratio $I_{2D}/I_G > 3$ for the exfoliated monolayer flakes, implying better quality for the HOPG within this study.

Graphene ribbons are obtained using electron beam lithography and a negative resist followed by oxygen plasma etch. After resist strip, the metal contacts are patterned using conventional electron beam lithography and metal lift-off. Since a large variation in wire length can mask the real device performance for this type of structures, reference samples are also processed in order to deduce the metal line contribution (Supplementary Information, Figure S1).

We used only one type of metal for contacts. Based upon literature reports combined with our in-house experimental results [15] we used 50 nm thick Pd as the contact metal. The contact resistance for Pd is one of the lower values reported today, as well as the metal is easy to process using standard lift-off processes. A summary graph on Rc ∗ W values obtained for different metal contacts to graphene from various works is provided in the Supplementary Information (Figure S2).

3. Results and discussion

Each sample (see also Fig. 1a–c) consists of a set of TLM structures varying in three parameters; the width of the graphene ribbon (W = 40 nm–1 μm), the channel length (L = 100 nm–10 μm) and the length of the contact (Lc = 100 nm–5 μm). From each TLM structure both the contact (Rc) and the sheet (Rs) resistance is extracted as a function of back gate voltage.

Typical R–Vg curves measured from a TLM structure are shown in Fig. 3a. Subsequently the different curves are aligned towards the neutrality point ($Vg - V_{NP} = 0$ V) and Rc and Rs are extracted by applying the TLM fitting formula for each gate bias (SI for full measurement

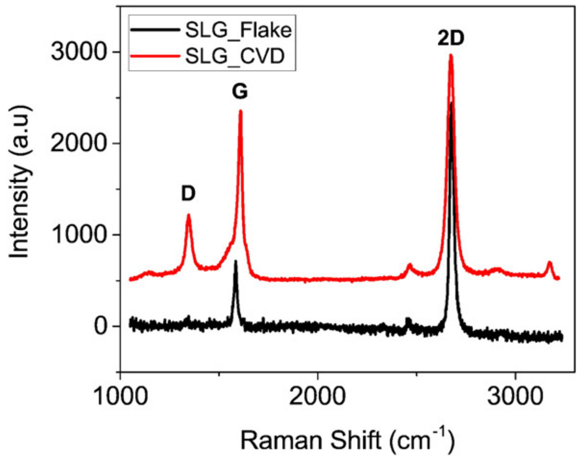

Fig. 2. Raman plots of the CVD and exfoliated single layer graphene. The absence of D-peak for the exfoliated graphene and the higher I_{2D}/I_G ratio compared to CVD is indicative of the currently higher quality of the exfoliated material in comparison to the synthetic one.