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Impact of technology scaling and process variations on RF CMOS devices

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Abstract

Inspired by the huge improvement in the RF properties of CMOS devices, RF designers are invading the wireless market with all-CMOS RF transceivers and system-on-chip implementations. In this work, the impact of technology scaling on the RF properties of CMOS; frequency properties, noise performance, linearity, stability, and non-quasi static effects is investigated to provide RF designers with an insight to the capabilities of future CMOS technologies. Moreover, the RF frequency performance of CMOS is investigated under the influence of process variations for different CMOS generations. Using the BSIM4 model, it is found that future CMOS technologies have high prospects in the RF industry and will continue challenging other technologies in the RF domain to be the dominant technology for RF transceivers and system-on-chip implementations.

Keywords: RF CMOS; Technology scaling; Process variations; Radio frequency; CMOS device

1. Introduction

Motivated by the significant CMOS performance improvements enabled by technology scaling [1,2], silicon CMOS is arising as a strong candidate for personal communication systems offering robust, high-density, high-performance, and low-cost system-on-chip implementations [3,4]. The performance of future CMOS technologies is expected to challenge that of bipolar implementations for RF applications. In the industry, CMOS performance improvements have enabled CMOS to be used almost exclusively in some applications such as Bluetooth [5], DECT [6], GPS [7], and WLAN [8].

In order to fully utilize the capabilities of CMOS in RF applications, circuit designers need to fully understand the impact of technology scaling on the RF performance of CMOS. In this paper, the RF performance improvement of CMOS devices is investigated for several Berkeley predictive CMOS technologies (70, 65, 45 nm) [9] and compared to some existing state-of-the art CMOS technologies (500, 350, 180, 130, 100 nm). The performance parameters investigated include: frequency performance, high-frequency noise performance, linearity, stability, and non-quasi static effects. Each parameter is analyzed to give the designers an insight about the impact of technology scaling on RF CMOS performance. In addition, with the growing threat posed by process variations in mind, the scaling of the impact of process variation with the technology is studied on the CMOS RF frequency figures of merit. To accurately model the increasing non-linearities of future nanometer CMOS devices, the BSIM4 model [10] is used to model all of the parameters under investigation.

This paper is organized as follows: In Section 2, the scaling trends of the CMOS parameters that directly affect the device RF performance are studied. The impact of technology scaling on the RF frequency response of CMOS is investigated in Section 3. The improvement in the noise performance of RF CMOS is depicted in Section 4. The linearity and stability of RF CMOS as technology scales down are analyzed in Section 5. A study of the onset of non-quasi static effects in RF CMOS and how it scales with the technology is presented in Section 6. The scaling of the impact of process variations on RF CMOS with the technology is studied in Section 7. Finally, the conclusions are drawn in Section 8.

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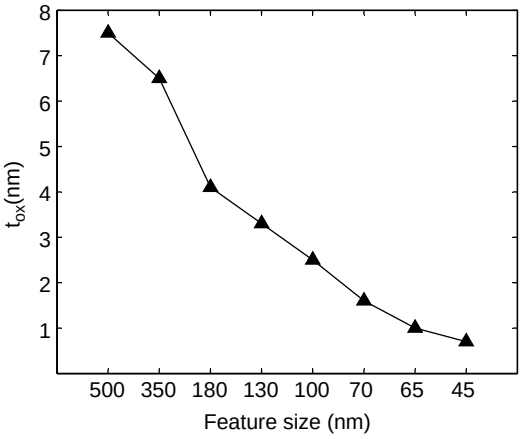

Fig. 1. Impact of technology scaling on t_{ox}.

2. Scaling trends of CMOS parameters relevant to RF design

As technology scaling continues to vigorously decrease the minimum feature size of the CMOS device, other CMOS parameters are scaled up or down accordingly to achieve higher performance. The main parameters that affect the RF performance of CMOS are: the oxide thickness t_{ox}, the total gate capacitance C_g, and the total gate resistance R_g. This section will study the scaling trends of these three parameters using the CMOS technologies under investigation.

2.1. Oxide thickness (t_{ox})

With the increasing demand on low-power RF circuits, the reduction of the supply voltage V_{DD} with technology scaling became a necessity. Moreover, reducing V_{DD} enhances the CMOS reliability by decreasing the electric field applied to the device gate. In order to speed up the CMOS operation as V_{DD} is reduced, the oxide capacitance t_{ox} is scaled down to lower the threshold voltage V_{th} with each technology generation in an effort to keep the ratio V_{DD}/V_{th} constant. In addition to V_{th}, the scaling of t_{ox} directly controls the scaling of the CMOS oxide capacitance C_{ox} and transconductance g_m. C_{ox} is inversely proportional to t_{ox} ($C_{ox} = \in_{ox}/t_{ox}$) and g_m is proportional to C_{ox}. Hence, both C_{ox} and g_m increase with technology scaling.

To investigate the impact of technology scaling on t_{ox}, the value of the oxide thickness is plotted for the CMOS technologies under investigation in Fig. 1 [9]. From Fig. 1, it is noticed that t_{ox} scales down with every technology generation by an average of 30%, thus giving new technologies larger driving capabilities and pushing them to higher speeds.

2.2. Gate capacitance (c_g) and gate resistance (r_g)

On the other hand, the CMOS parasitics, gate capacitance C_g and gate resistance R_g, increase with each technology generation. In Fig. 2(a) and (b), the scaling trends of C_g and R_g, respectively, are plotted for the technologies under investigation. It is noticed that the average increase in C_g and R_g is 15 and 25%, respectively, with each technology generation. The increase in these CMOS parasitics limits the improvement in the performance of CMOS devices with scaling.

3. Impact of technology scaling on CMOS frequency response

The RF frequency figures of merit of the CMOS device are: the cutoff frequency f_t, the maximum oscillation frequency f_{max}, and the maximum gain G_{max}. The scaling trends of the CMOS RF frequency figures of merit is investigated using the technologies under investigation.

3.1. The cutoff frequency (f_t)

The cutoff frequency f_t is defined as the frequency at which the current gain of the device is unity. For a CMOS

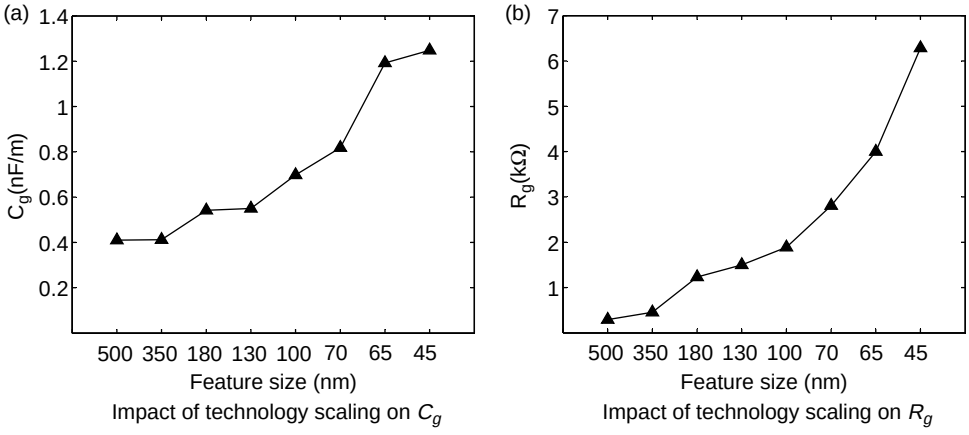

Fig. 2. Impact of technology scaling on CMOS parasitic capacitance and resistance.