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A chemical mechanical planarization model for aluminum gate structures

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ABSTRACT

In this work, we propose a new aluminum gate chemical mechanical planarization (CMP) model to describe the metal gate height variation in 32 nm high-k metal gate (HKMG) process based on chemical kinetics and contact mechanics. The effects of mechanical abrasion, concentration of different types of chemical reagents and hydrogen ions, pattern geometry and pad elastic properties on surface profile are physically captured. In the process of constructing the model, the discrete convolution and fast Fourier transform (DC–FFT) technique is integrated with conjugated gradient method (CGM) for calculating the contact pressure between the wafer surface and the polishing pad. Then the computed pressure distribution is introduced into the new constructed chemical kinetics formula to determine the local removal rate of the underlying patterns and predict the evolution of the wafer surface topography. The detailed relationship between the metal gate dishing post-Al-CMP and the design pattern structures are systematically investigated. The model agrees reasonably well with the experimental data measured from the HKMG test structures. Therefore, it can be utilized for quantifying the effect of pattern geometry on dishing, predicting the wafer surface height evolution and optimizing some design rules for manufacturability to improve the surface planarization of HKMG structures.

1. Introduction

In modern integrated circuits (ICs), chemical mechanical planarization (CMP), adopted by semiconductor industries has become one of the most important solutions for surface global planarization and generated new possibilities for the development of innovative semiconductor manufacturing processes. It is a critical process in which material is removed from the wafer before the next layer of the IC is constructed. CMP has its roots in the glass polishing industry and then is employed into the semiconductor manufacturing because of its ability to produce flat surfaces with low levels of roughness. However, the tolerances needed for the semiconductor application are obviously more stringent and challenging during the fabrication of fin field effect transistor (FinFET) devices [1,2], in the replacement metal gate (RMG) technique for high-k metal gate (HKMG) structures [3], in creating shallow trench isolation (STI) structures [2], damascene metallization [4] and in the processing of microelectromechanical systems (MEMS) [5], causing CMP to be a heavily studied process [2,6–14].

The material removal rate (MRR) which is the most important topics of the modeling during CMP process depends sensitively on chemical slurry components, applied pressures, polishing pads, abrasive particles and pattern geometry effects. Predicting MRR is challenging because of the complex interplay between chemical and mechanical processes. In order to capture the chemical behavior and describe the repetitive removal of the wafer profile variation, the steady-state surface kinetics model is an elegant approach to relate the overall polish rate to various kinetic processes occurring at the surface modulated by the mechanical parameters [15–20]. The kinetics model can successfully capture the polish rate with experimental data for different oxidizers, abrasives, and polishing conditions. Meanwhile, mechanic-based models have been widely proposed to elucidate the mechanical aspects of the polishing process. Different kinds of scale models using contact mechanics or fluid hydrodynamics with mass transport model attempt to develop an understanding of the various phenomena occurring at different length scales. Wafer scale models are usually concerned with the pressure distribution describing the direct contact incorporating wear mechanisms to predict the variation of removal rates among abrasive particle, pad asperity, and wafer surface [12,15,21,22]. Combined with the Navier Stokes equation and mass transport equation, the mixed lubrication model taking into account the compressibility of the pad and the mold of slurry delivery [23] is used to give reasonable predictions of the pressure profiles and removal rates [15,24–26].

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Otherwise, several active particle models, decoupled from the prediction of the MRR, are investigated [27]. During CMP, the non-Prestonian behavior could be modeled using a modified version of active particle model [11] and a diffusion model to capture the effect of the slurry chemicals [28]. A new material removal method [29] based upon the formation of a modified wafer surface layer due to the chemically-active slurry and a statistical model which introduces Bayesian analysis to predict the CMP performance are developed [30]. To predict the effect of slurry parameters on MRR, a novel CMP model was introduced to predict the total number of abrasive particles removing material by calculating the number of particles on single pad asperity, assuming a uniform distribution of particles in the slurry, and multiplying the result by the total number of pad asperities in contact with the wafer [31]. At the same time, when grain flow approximation was applied to lubrication theory, the film thickness and shear stress can be predicted [32]. By balancing forces and moments on the wafer, the number of particles taking part in the material removal can be related to the concentration of the slurry and the pad groves which are utilized to predict the interfacial fluid pressure are also taken into account [33]. Combinations of cosine functions to extrapolate finite element analysis results for the contact stress to various scenarios encountered during CMP are introduced to predict the effect of wafer topography [34]. A deterministic semi-analytical model for investigating the elastic contact between a rough bi-layer porous body (pad) and a rigid plane (wafer) was also presented [35]. In these studies, it is seen that the different contact pressure at different areas between the wafer and the pad is the key reason for the removal rate nonuniformity. The contact pressure distribution is greatly affected by the complex surface topography including the pattern features on the wafer surface. Moreover, both chemical and mechanical components of CMP are used to capture the material removal mechanisms from the wafer surface by process and separate kinetic parameters on a fundamental level [36].

Although the material removal rate has been extensively investigated from different perspectives and scales, the CMP process is still not fully understood. The reason is that, in spite of its apparent simplicity, CMP is really a quite complicated process in which both mechanical and chemical factors play an important role on the surface planarity. CMP may result in excessive erosion of the dielectric layer or dishing of metal lines if the process is not properly controlled, which will severely influence the depth of focus in lithography process. Since the surface topography of a wafer after CMP process step has a significant impact on wafer yield, numerous attempts have been made to predict the evolution of the wafer surface during the polishing process [15,37–43].

The chip-scale models [44–48] is one of the representative investigations which have been used to predict the pattern dependence, optimize the functionality of the circuit and modify the chip design in the context of design for manufacturability. These efforts are largely built on a phenomenological basis and provide less physical and chemical insight in the actual CMP process [15]. Feature scale models attempt to describe and predict how individual features on a wafer evolve during the polishing process. Many research works have used the fluid-based wear model [49] and contact mechanics [36,42,50] to analyze the pressure distribution and surface height evolution. When the pad contact completely with both up area and low area, a step height reduction model was proposed in which pad is assumed to behave like a linear elastic spring [51]. The metal dishing and dielectric erosion of the feature structure are investigated as a function of wafer pattern geometry. By considering the compliance of the polishing pad as well as its roughness, the individual pad asperities and the pattern characteristics play an important role on describing the final surface topography [15].

As the semiconductor industry scaling down to nanometer technology node, the process and materials in the integration are pushed to the limit. Further scaling down of the oxide thickness to achieve faster device performance is impractical due to fundamental limitations [52,53]. The introduction of HKMG which adopts a RMG approach lower than 45 nm technology node for CMOS process promises to enable conventional scaling of the transistor as well as reduced stand-by power. The HKMG combination is important for the emerging applications that require high-performance and low gate-leakage including all silicon and non-silicon nanoelectronic transistors (III-V materials, carbon nanotubes) [54]. It has been adopted by most of IDM and foundries due to its associated lower thermal budget, more stable threshold voltage, and improved performance from strain induced dummy gate removal than the alternative gate-first approach. Poly opening polishing (POP) CMP processing before dummy poly removed and Al-CMP implementation after work function metal deposited, have been developed to fabricate the HKMG products [55]. Compared with the conventional CMP process, the dimensional tolerance of Al-CMP is more challenging for its narrow metal gate layer. In a HKMG structure, the contact of different materials (from the galvanic series) is a matter of serious concern in the CMP process of such structures [56,57]. Moreover, the control of the metal gate height uniformity and defectivity, including micro scratch and corrosion defect types in Al-CMP process is also quite crucial to influence the device and yield performance of HKMG structures [58–67].

The gate height is critical to transistor performance and precisely controlling the gate height and uniformity is the primary challenge for the HKMG Al-CMP process. Non-uniform gate height can cause gate resistance variation, and improper gate heights can result in subsequent contact etch problems. Aluminum CMP is used to remove the Al overburden and work function metals from the field after Al gap fill. The gate height is only several hundreds of angstroms and the size of aluminum line is quite thinner, so Al-CMP process tolerance is much tighter. This places extremely tight within-wafer (WIW) and wafer-to-wafer control on the Al polishing to meet the gate height uniformity requirements. Therefore, how to control the removal rate and surface roughness has received much attention in HKMG Al-CMP process [65–67].

Up to now, although a large number of CMP models have been proposed, many fundamental effects of chemical reagents on the material removal are not well formulated systematic mathematical models to adequately describe the process mechanism for HKMG structures. Therefore, in order to obtain a good HKMG Al gate surface planarity, chemical and physics-based model is quite helpful in providing fundamental insight on the evolution of the gate profile, optimization the process, and implementing CMP design rules [66].

In this paper, a new chemical and mechanical synergistic Al-CMP model has been explored to systematically govern the combinational effects of mechanical abrasion and chemical reactions in HKMG CMP process. Based on the chemical kinetics and contact mechanics, the new formula of aluminum material removal rate is constructed and introduced into the wafer surface topography simulation. To verify the present CMP model, a set of test structures is designed abiding by the nanometer IC design rules and polished under the same production process condition except for different polishing wafers. Part of the test structures are applied for model parameter extraction and the rest of the data are utilized for model verification. After validated by the experimental data, the model is further used to simulate another set of structures for surface dishing prediction. Considering the application of the present model for Al-CMP process, it can be used to optimize some basic design rules for the surface evolution control in HKMG CMP process.