Microelectronic Engineering 110 (2013) 141–146

Contents lists available at SciVerse ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Patterning of Si nanowire array with electron beam lithography for sub-22 nm Si nanoelectronics technology

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ARTICLE INFO

Article history:
Available online 19 March 2013

Keywords:
Electron beam lithography
Lithography/etching interaction
Inter-pattern electrostatic repulsion
Nanowire patterning
Hydrogen silsesquioxane (HSQ)
Diluted electron beam resist

ABSTRACT

In order to form practical arrays of Si nanowires narrower than 22 nm using electron beam lithography (EBL) with hydrogen silsesquioxane (HSQ) resist and reactive ion etching (RIE) process with inductively-coupled plasma, a new type of lithography/etching interaction is studied. The inter-pattern electrostatic repulsion appears to determine the patterning limit to be 28 nm while causing the RIE dummy patterns to collapse. Approaches to reduce the electrostatic force on the RIE dummies are tried from design and process perspectives. Designing additional dummy patterns next to the RIE dummies and fixing pattern-to-pattern distance to be 70 nm are tried. Another efficient approach is to use thinner HSQ resist to reduce the repulsion among patterns. Here we confirm that the nanowire patterns narrower than 20 nm can be formed by using diluted HSQ solutions.

1. Introduction

Due to the aggressive scaling-down of the feature sizes in microelectronics technology and the resolution limit of 193 nm ArF-based patterning technologies, employment of non-optical next generation lithography (NGL) is near [1–3]. According to the 2011 edition of the international roadmap for semiconductor, there are no proven solutions for optical lithography after the technology nodes beyond 22 nm [4]. Predicted future lithography technologies for now are reported to be extreme ultraviolet (EUV) lithography [5,6], nano-imprinting [7], directed self-assembly (DSA) [8], and mask-less lithography (ML2) represented by the electron beam lithography (EBL). Among these NGL candidates, EBL is an attractive option in that the wavelength of the beam is picometer-scale; there is no need of complex mask making; the cost of ownership is relatively low compared to that of the EUV lithography; and the throughput continues to improve [9–15]. However, the problems caused by the charge nature of the beam such as proximity effect and beam broadening have required the users to have additional considerations on electrostatic interaction [11]. In addition, because of the scaling-down of pattern-to-pattern space as well as line width [16], this electrostatic effect will become a more serious issue. Therefore, a new type of the lithography/etching interaction issue is expected to degrade the resolution limit. In this sense, investigating the EBL/etching interaction and preparing proper solutions to handle it will be of a great practical importance for EBL technique to remain as a competitive NGL option applicable to sub-22 nm Si nanoelectronics technology.

This work begins with the investigation on the limit of patterning and the new type of EBL/etching interaction in the conventional EBL technique. After that, the techniques to overcome the issues caused by the electrostatic interaction are studied from design and process perspectives. Patterns to form nanoelectronic devices are used instead of periodic line-and-space patterns to study the practical cases in microelectronics fields.

2. Experiments and materials

For the preparation of materials and test, the microelectronics fabrication facilities located at Seoul National University and Korea Advanced Institute of Science and Technology in Republic of Korea were used. With an electron beam direct writer of JEOL Ltd. (model: JBX-6300FS), patterns in GDS file format generated by Cadence Virtuoso layout tool were imaged onto negative EBL resist film of hydrogen silsesquioxane (HSQ) over a stack of target films. The EBL resist film was prepared from a commercial methyl isobutyl keton (MIBK) solution of HSQ (product name: XR-1541-006, Dow Corning Co.) by spin-coating at 5000 rpm and soft-bake at 120 °C. As for the exposure, an areal Gaussian beam of 2.2 nm in diameter was used with 4 nm of beam step size and a single-pass writing strategy. The acceleration energy and the beam current were set

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0167-9317/$ - see front matter
http://dx.doi.org/10.1016/j.mee.2013.03.023

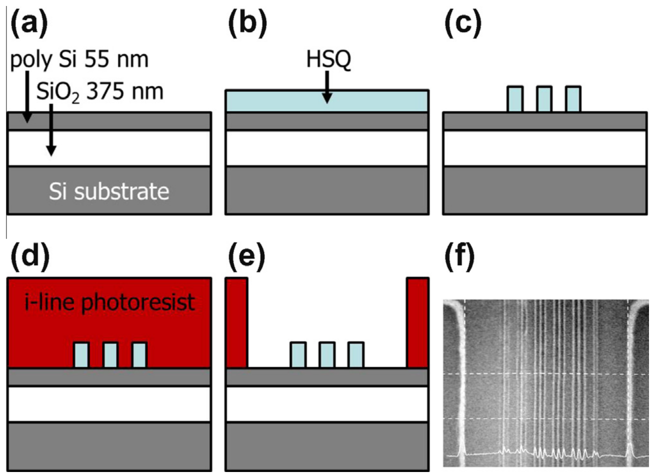

Fig. 1. Process flow to form the structure of the film stack just before RIE process: (a) deposition of LP CVD poly Si and high-density plasma CVD SiO_2, (b) HSQ layer formation, (c) nano-line resist pattern formation, (d) photoresist layer coating and soft-bake, (e) i-line pattern formation, and (f) in-line SEM image of patterns before RIE process. Here, the thicknesses of poly Si and SiO_2 of the process monitoring wafers were confirmed from five-point ellipsometry measurement before HSQ coating and the standard deviation of the measurements was less than 3% of the average value across the wafer. Five-point photoresist thickness after hard bake was 896.4 nm in average with a standard deviation of 1.86 nm.

to be 100 keV and 1 nA respectively to maximize the resolution. The imaged HSQ film was developed in a commercial tetramethyl ammonium hydroxide developer (product name: MICROPOSIT MF-312, Shipley Co.) and baked at 190 °C. After the complete HSQ-based EBL process, optical photolithography with an i-line photoresist based on phenol–formaldehyde resin (product name: SS03A9, Dongwoo Fine-chem Co., Ltd.) was performed as "mix-and-match" process to make it easier to find inspection points (Fig. 1). The film stacks with the masking patterns were etched in an inductively-coupled plasma reactive ion etcher of Lam Research Co. (model: TCP9400DFM) with gas chemistry based on the mixture of hydrogen bromide, chlorine and oxygen [17]. Two-step time-based reactive ion etching (RIE) process composed of oxide break-through and main-etch steps were set up after monitoring the change in the optical spectrum of plasma during etching process. The organic photoresist was removed in oxygen plasma environment of an asher of TePla AG (model: 300). As-develop and as-etch profiles of patterns were examined with in-line inspection and analytical scanning electron microscopes of Hitachi High Tech Co. (S-8820 and S-48000, respectively) Fig. 1 schematically illustrates the process flow and film stack just before RIE process. As a target film to form nanowire with, poly-silicon layer of 55 nm was deposited at 625 °C by low pressure chemical vapor deposition over silicon oxide of 375 nm. The thicknesses of the films were confirmed from the monitoring wafers of the same processes. The silicon oxide layer worked as a stop layer to etch the silicon layer. The film stack was intended to simulate the stack of silicon-on-insulator (SOI) substrate.

3. Results and discussions

3.1. Si nanowires formed by a conventional EBL technique

First, the limit of EBL process with the explained practice was investigated while changing electron beam dose. Since it is well known that the RIE loading effect tends to make the isolated patterns more sloped and most patterns in nanoelectronics are drawn in nested designs, we try to find the optimum EBL condition for arrayed nanowire patterns of various widths with the dose varied from 600 to 1900 $\mu C/cm^2$. Fig. 2 shows the as-develop images of 26 nm-wide nanowire arrays. A dose below 1000 $\mu C/cm^2$ was not enough to form nanowire patterns of 30 nm and below. Unwanted resist footing started to appear once the dose exceeded 1300 $\mu C/cm^2$. Therefore, the optimum electron beam dose seemed to be between 1000 and 1300 $\mu C/cm^2$. With the optimum dose, the arrays of 24 nm-wide nanowires were printable.

Next, after confirming the electron beam dose window from the as-develop inspection data, isolated triple-line patterns were examined. The reason to examine triple lines instead of single lines was because completely isolated single lines are not used in

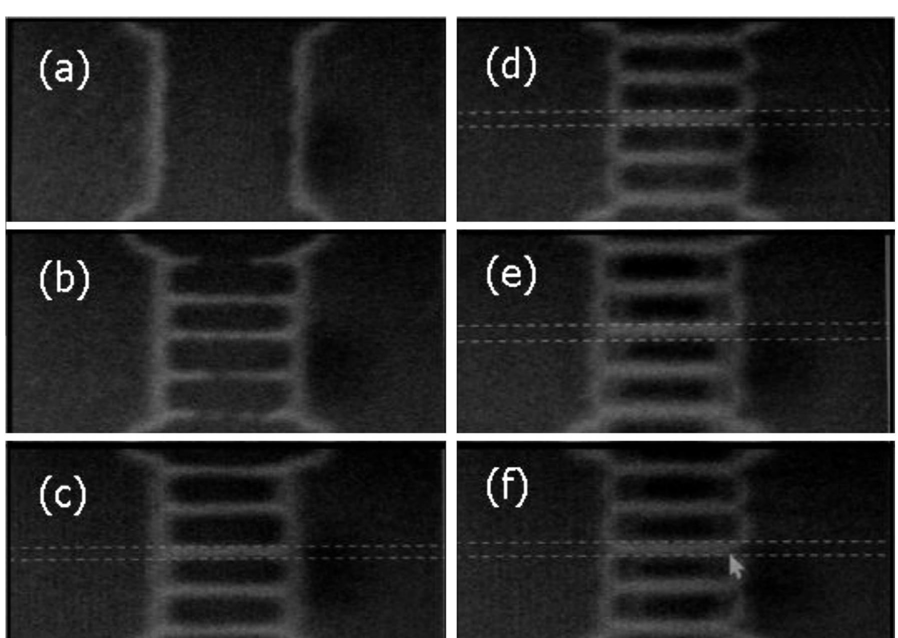

Fig. 2. As-develop inspection images of nanowire arrays with different electron beam dose conditions. Each conditions are (a) 600, (b) 800, (c) 1000, (d) 1300, (e) 1500, and (f) 1900 $\mu C/cm^2$.