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Study of etching bias modeling and correction strategies for compensation of patterning process effects

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ABSTRACT

In addition to simulating lithography process effects, process models must accommodate pattern distortion due to the etching process. An etching bias modeling method and a staged correction strategy have been developed to compensate for such patterning process effects efficiently. However, the staged correction strategy may cause inaccurate compensation of patterning process effects since the patterns used to simulate etching process effects are assumed to be rectilinear. In fact, the patterns will be distorted during the lithography process. Therefore, a promising correction strategy that incorporates a recently developed optical proximity correction algorithm is proposed to deal with this problem. It can compensate for lithography and etching process effects simultaneously. In order to conduct this study, the etching bias modeling method is investigated by rigorous process simulations. The resulting model provides a reasonable fit to the measured data from the process simulations and can simulate etching process effects reasonably well. The performance of the proposed correction strategy in terms of correction accuracy and run time is examined. Numerical experiments show that the correction accuracy obtained is significantly improved compared with that obtained by the staged correction strategy. However, the total run time required is increased by a factor of ~2.5, which is practically acceptable for full-chip correction.

1. Introduction

As the device dimensions continue to shrink, tight control of critical dimension (CD) errors over the patterning processes becomes increasingly important. Consequently, it demands more accurate practice of model-based optical proximity correction (OPC). During the model-based OPC process, a process model is invoked to adjust the mask pattern iteratively so that the final pattern transfer to the wafer is as close as possible to the drawn pattern. It has been demonstrated that in addition to simulating lithography process effects, process models must accommodate pattern distortion due to the etching process [1]. While the etching process may be lumped with the lithography process into one process model, it can no longer be considered as a small perturbation on lithography process effects [2]. Therefore, it is required to develop nonlinear model formulations that differ from the convolution based process models used to simulate lithography process effects [1,3].

An etching bias modeling method that uses nonlinear components in combination with conventional convolution kernels has been developed for simulating etching process effects [3–5]. In the meanwhile, a staged correction strategy, as shown in Fig. 1, has been developed to deal with the patterning process models which are calibrated separately (i.e. the etching bias model and the process model) [2,3,6]. The concept of the staged correction strategy is to perform a series of discrete inverse transformations on the drawn pattern, where the drawn pattern is the input and target for compensation of etching process effects, and the resulting output becomes the target or input for compensation of lithography process effects. The accuracy of etching bias modeling and the staged correction strategy have been verified using the 45 nm process data collected from the Interuniversity Microelectronics Center [7,8], and the performance of etching bias modeling with multiple layers has been demonstrated [9]. This state-of-the-art correction strategy usually requires two stages of fine-tuning of control parameters in order to achieve proper convergence and can compensate for patterning process effects efficiently.

However, the patterns used to simulate etching process effects are assumed to be rectilinear. In fact, the patterns will be distorted during the lithography process, such as line end shortening, corner rounding, and line edge roughness. This assumption may cause inaccurate compensation of patterning process effects, resulting in the deviation of the electrical characteristics of the circuit from the design intent [10]. Therefore, a promising correction strategy that incorporates a recently developed OPC algorithm [11] is proposed to deal with this problem. The performance of the proposed

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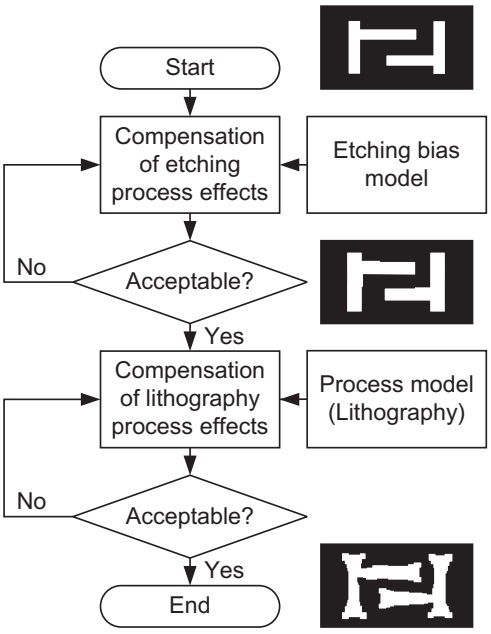

Fig. 1. Staged correction flow.

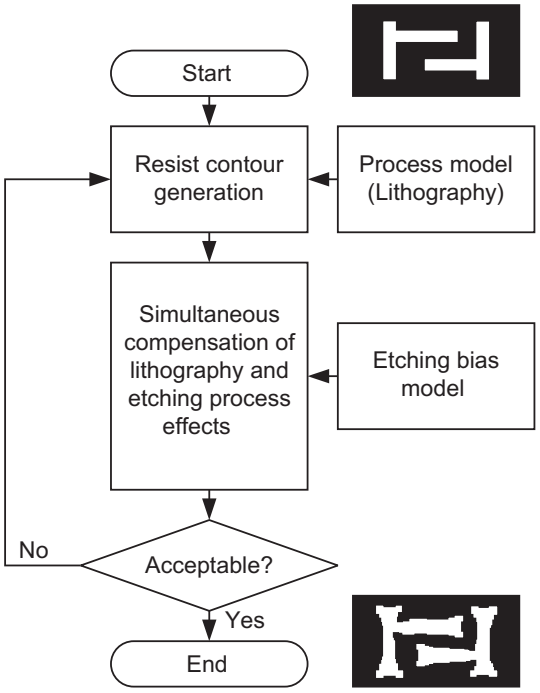

Fig. 2. Proposed correction flow.

correction strategy in terms of correction accuracy and run time is explored using the etching bias model built in this study.

Numerical experiments are designed according to the 38 nm half-pitch node reported in the International Technology Roadmap for Semiconductors (ITRS) [12]. Standard logic cells used in this study are scaled down to the 38 nm half-pitch node [13], where the minimum CD and pitch for the first metal layer are 38 and 76 nm, respectively. The rest of this paper is organized as follows. Section 2 presents the concept of the proposed correction strategy. Section 3 investigates the etching bias modeling method using rigorous process simulations. Section 4 shows the results of numerical experiments, followed by the conclusions in Section 5.

2. Proposed correction strategy

A promising correction strategy that incorporates a recently developed OPC algorithm [11], as shown in Fig. 2, is proposed to compensate for lithography and etching process effects simultaneously. The recently developed OPC methodology, called non-delta-chrome OPC (non-DCOPC), does not require the iterative computation of the mask perturbation used in the conventional OPC methodology [11]. Prior to the correction, the dissection process is performed based on the minimum segment length ($L_{\min}$) to form small movable segments along polygon edges of the drawn pattern, and an evaluation point is assigned to each movable segment. During the correction process, the resist contour is generated from the mask pattern and using a process model. The image intensity of the resulting resist contour is then computed using an etching bias model. The correction amount is calculated from the intensity error (IE) values and using the proportional-integral-derivative (PID) control method. The IE is the difference between the image intensity and the threshold at the evaluation point. Each segment of the mask pattern is then moved by the correction amount. The correction process will cease when the edge placement error (EPE) for each segment is within an acceptable range of tolerance.

Using the PID control method, the correction amounts can be computed as follows:

$$\begin{aligned}\mathbf{u}_j &= \mathbf{u}_{j-1} + K_{\mathrm{p}}(\mathbf{e}_j - \mathbf{e}_{j-1}) + K_{\mathrm{i}}\mathbf{e}_j + K_{\mathrm{d}}(\mathbf{e}_j - 2\mathbf{e}_{j-1} + \mathbf{e}_{j-2}) \\ &= \mathbf{u}_{j-1} + (K_{\mathrm{p}} + K_{\mathrm{i}} + K_{\mathrm{d}})\mathbf{e}_j - (K_{\mathrm{p}} + 2K_{\mathrm{d}})\mathbf{e}_{j-1} + K_{\mathrm{d}}\mathbf{e}_{j-2},\end{aligned} \tag{1}$$

where $\boldsymbol{u}_j$ is the vector of correction amounts at the j'th iteration, $\boldsymbol{e}_j$ is the vector of IE values at the j'th iteration, K_{p} is the proportional parameter, K_{i} is the integral parameter, and K_{d} is the derivative parameter. In order to achieve convergence in a reasonable time, it is important to tune the values of K_{p}, K_{i}, and K_{d}. A heuristic tuning method to achieve convergence is adopted. The fundamental idea of this tuning method is to develop the rules based on trial-and-error learning. The values of K_{p}, K_{i}, and K_{d} are adjusted heuristically until the convergence criterion is achieved by showing that if there exists J such that

$$\exists j < J \Rightarrow \|\varepsilon_j\|_\infty \leqslant \alpha, \tag{2}$$

where J is the maximum number of iterations, $\boldsymbol{\varepsilon}_j$ is the vector of EPE values at the j'th iteration, and α is a small number that allows the approximate EPE value to bounce within an acceptable range of tolerance.

Fig. 3 shows the non-DCOPC algorithm, where, $\boldsymbol{u}_j$ is round to a multiple of the grid size (δ), and the drawn and corrected layouts can be in either a GDSII (graphic data system II) or OASIS (open artwork system interchange system) format. The proposed correction strategy is implemented in a commercial OPC tool [14]. It is demonstrated that the process of generating contours requires a substantial computing time. Iterative adjustments to the mask pattern are made during the correction process. If the number of iterations required for convergence can be reduced, the increase in the total run time over the staged correction strategy can be reduced. The proposed correction strategy, unlike the staged correction strategy, requires only one stage of fine-tuning of control parameters for achieving proper convergence.

3. Etching bias modeling and calibration

In order to conduct this study, the etching bias modeling method [3,5] is investigated by rigorous process simulations. The oxide etching process is simulated by a commercial technology computer-aided design tool [15]. All simulations are performed on a computer with two 2.27 GHz quad-core Intel Xeon E5520 central processing units and 96 GB of main memory. The simulation