Microelectronic Engineering 110 (2013) 230–233

Contents lists available at SciVerse ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Fabrication of bulk and epitaxial germanium field emitter arrays by dry etching techniques

S. Carta [a], R. Bagni [b], E. Giovine [a], V. Foglietti [a], F. Evangelisti [b], A. Notargiacomo [a,*]

[a] CNR – Institute for Photonics and Nanotechnology, Via Cineto Romano 42, 00156 Rome, Italy
[b] Physics Department "E. Amaldi", Università degli Studi Roma TRE,Via della Vasca Navale 84, 00146 Rome, Italy

ARTICLE INFO

Article history:
Available online 12 December 2012

Keywords:
Reactive ion etching
Epitaxial semiconductor
Field emission array
Electron beam source

ABSTRACT

We present the fabrication and characterization of novel high density field emitter arrays (FEAs) on CVD-grown epitaxial germanium on (001) silicon. In particular we propose a heterostructure made up of silicon as substrate and of germanium as active layer, exploiting the infrared transparency of Si and the infrared sensitivity of Ge to realize a semi-transparent photo-assisted electron beam source. We used a completely dry etching process in fluorinated gases (SF_6) due to its significant under-etching for both silicon and germanium. High aspect ratio silicon and germanium FEAs, with minimum tip radii of 25 nm and 40 nm, respectively, and lower aspect ratio Ge/Si FEAs with minimum tip radii of 50 nm were fabricated. The realized FEAs show good emission behavior with field emission characteristics straight related to tip geometry: low electric field threshold for silicon and germanium tips (<18 V/μm) and enhancement factor of more than 250 and 130, respectively; conversely for the epitaxial germanium we obtained 32 V/μm for electric field threshold and 70 for enhancement factor. Current emission time stability for silicon, for germanium and for Ge/Si field emitter arrays were demonstrated.

1. Introduction

Many types of electron beam sources were developed for use in electron microscopy and lithography, for ultrafast laser shape diagnostic in streak cameras, for X-ray generation, for high energy physics experiments and commercial displays. High emission current density, high brightness, high time stability and long lifetime are the most important requirements for electron beam sources [1]. Hot cathodes, based on thermionic effect, and cold cathodes, based on photoemission or field emission mechanism are usually employed. In particular, semiconductor-based material can be employed for high quantum efficiency photocathodes and photo-sensitive field emitters. Semiconductor single tip field emitters are extensively used as optical stimulated beam sources to reach high peaks emission current [2]. However the most limiting factor of single tip emitters is the overheating at high operating current with destructive effect and remarkable current fluctuation. To overcome overheating effect preserving high peak emission current, large area semiconductor field emitter arrays (FEAs) are the most attractive devices for electron beam guns [3]. *p-type* silicon FEAs exhibit excellent dark and photo-sensitive field emission properties [4] up to $\lambda \sim 800$ nm wavelength light source. Germanium can be able to shift photo-sensitive region up to $\lambda \sim 1550$ nm and can be employed in silicon technology to realize large area FEAs. Thus mixing the transparency properties of silicon for wavelength greater than ~1 μm and the photo-sensitive of germanium up to $\lambda \sim 1550$ nm, it is possible to realize a semitransparent photo-field emitter at $\lambda \sim 1550$ nm.

The conventional silicon FEAs fabricated by a two step process, namely wet or dry etching and oxide sharpening, cannot be applied to germanium since Ge does not allow the formation of the thermal oxide needed for achieving high aspect ratio tips. Due to the poor control over the wet etching of Ge, we have thus proposed a totally dry etching process to realize innovative epitaxial germanium FEAs.

2. Materials and methods

The fabrication of epitaxial germanium FEAs required the characterization and optimization of the etching step on bulk silicon and on bulk germanium first, and the final transferring of the process to epitaxial germanium.

2.1. Materials used

Two kinds of substrates were used: (a) 1–10 Ω·cm, *p-type* (001)-oriented, 650 μm thick Si wafers and (b) 0.1–1 Ω·cm, *p-type* (001)-oriented, 400 μm thick Ge wafers.

* Corresponding author. Tel.: +39 0641522271; fax: +39 0641522220.
E-mail addresses: stefano.carta@ifn.cnr.it (S. Carta), roberta.bagni@gmail.com (R. Bagni), ennio.giovine@ifn.cnr.it (E. Giovine), vittorio.foglietti@ifn.cnr.it (V. Foglietti), evangelisti@fis.uniroma3.it (F. Evangelisti), notargiacomo@ifn.cnr.it (A. Notargiacomo).

0167-9317/$ - see front matter
http://dx.doi.org/10.1016/j.mee.2012.11.024

The epitaxial germanium used in this work is grown in dedicated CVD chamber with entire control of thickness and doping [5].

After wafer dicing along (001) direction, $1 \times 1\ cm^2$ chips were degreased in ultrasonic bath in acetone followed by isopropanol.

2.2. Device fabrication

In order to realize silicon field emitter array, 50 nm aluminum etch mask was patterned by electron beam lithography and lift-off. PMMA electronic resist was spin-coated and post baked at 170 °C for 5 min resulting in a 600 nm thickness. Several arrays of squares of different size were patterned with 20 μm pitch. After aluminum thermal evaporation and lift-off, the silicon chip is introduced in RIE chamber for etching.

First, oxygen plasma (196 sccm flux, 100 mTorr pressure for 60 s at 56 mW/cm^2 RF power density) is used for surface cleaning from resist residuals; then CHF_3 plasma (100 sccm flux, 50 mTorr pressure for 20 s at 288 mW/cm^2 RF power density) is used to etch away the silicon native oxide layer that could inhibit the following silicon etching in SF_6. Finally we used low pressure and low RF power SF_6:O_2 plasma (SF_6 flux of 26 sccm and O_2 flux in the $0 \div 16$ sccm range, 30 mTorr pressure for 20 s at 75 mW/cm^2 RF power density) to obtain good silicon etching isotropy. The etching process was tailored using different percentage of O_2 and variable etching time. In order to maximize the tips aspect ratio, we maximized the vertical to horizontal etch rate ratio: while in pure SF_6 the ratio is 2 we obtained a ratio of up to 4.5 by adding 16 sccm of O_2, and a correspondent vertical etch rate of 250 nm/min. For each dimension of the masks, several identical arrays were separately etched in order to find the correct etching-time such that the aluminum square mask above the formed tip just fell down. The establishment of the etch time is critical since lower etching-time produced truncated pyramids with flat top, whereas over-etching produced less sharpened tips.

After dry etching process, resist and aluminum mask residuals were removed in acetone followed by HF diluted solution. Arrays of 50×50 9-μm wide square masks after ∼30 min etching produced hyperbolic pyramids, 10 μm high, 20 μm spaced, with tip radii of 25 nm, on a $1 \times 1\ mm^2$ area, as shown in detail in Fig. 1a. The octagonal shape of the pyramid base is shown in the top-view SEM picture of Fig. 1b, and is originated by the undercut at mask corners as found in conventional anisotropic silicon wet etching [6].

In order to realize germanium field emitter array, we first transferred silicon etching process to germanium substrate without any process parameter modification. We used circular and square masks to fabricate cones and pyramids, respectively. By using the same gas mixture employed for silicon, we observed that germanium vertical etching is ∼6× faster however essentially maintaining the same vertical to horizontal etch rate ratio, i.e. ∼4. Fig. 1c and d shows square- and circle-masks arrays, respectively, before the complete formation of the tips: square-top truncated pyramids (c) and octagonal-top truncated cones (d) are produced.

Unlike silicon etching process where the greater lateral etching rate takes place at the separation surface between metal mask and semiconductor, in germanium lateral etching occur faster at a certain depth below the mask level: thus the tip formation can take place well below the surface.

The total height of the tip, keeping constant etching time, depends dramatically on the mask shape and size: in fact, unlike for the case of square masks, the curved edge of circular masks tends to favor the underetching thus leading to a faster formation of the tip, and to the appearance of several etch-stable lattice-planes producing the typical octagonal shape, as shown in Fig. 1d.

After aluminum removal, the germanium FEAs produced using the above described etching process had tip radii ∼40 nm (Fig. 2a).

Despite of the large difference in the lateral etch rate of bulk Ge respect to bulk Si, that is of the order of 6× as described above, the

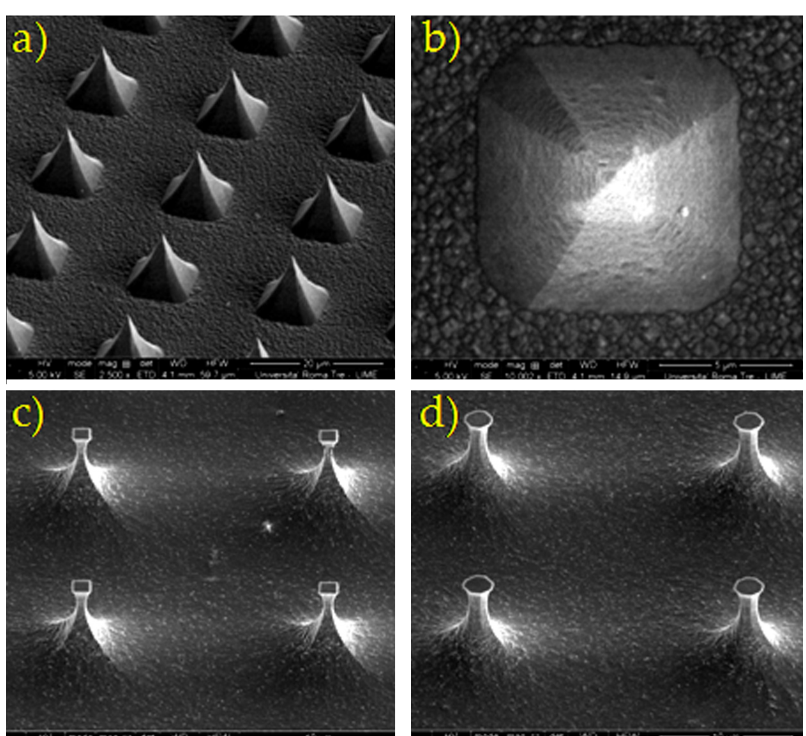

Fig. 1. (a) hyperbolic pyramid silicon field emitter array realized by RIE process; (b) plan view showing the octagonal base due to underetching at mask corners; (c) hyperbolic pyramid and (d) cone germanium field emitter arrays with tips not yet formed.