Microelectronic Engineering 97 (2012) 59–63

Contents lists available at SciVerse ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Nanostructuring of silicon substrates for the site-controlled growth of GaAs/$In_{0.15}Ga_{0.85}As$/GaAs nanostructures

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ARTICLE INFO

Article history:
Available online 30 March 2012

Keywords:
Nanostructuring of silicon
Electron beam lithography
ICP dry etching
MBE growth
InGaAs quantum dots

ABSTRACT

We report the optimization of electron beam lithography and inductively coupled plasma (ICP) dry etching processes to fabricate pre-patterned Si (100) substrates with sub-100 nm holes with controlled size and shape. An efficient in situ cleaning sequence based on atomic hydrogen cleaning at 500 °C combined with thermal oxide desorption at 750 °C confirmed by reflection high energy electron diffraction (RHEED) pattern of two dimensional clean surface prior to the MBE growth has been established. The MBE growth of GaAs/$In_{0.15}Ga_{0.85}As$/GaAs system on patterned Si surface has shown highly selective formation of localized dome like nanostructures in patterned holes with 1 μm period.

1. Introduction

Silicon is the main material in the microelectronic industry due to its excellent electronic, thermal and mechanical properties. However due to its indirect band gap silicon exhibits poor optoelectronic properties. On the other hand, group III/V materials have excellent optoelectronic properties due to their direct band gap. Efficient optical devices based on epitaxially grown III/V low dimensional structures such as In(Ga)As quantum well and quantum dots (QDs) on GaAs substrate have long been established. The integration of III/V optoelectronic devices with silicon electronic circuits could bring enormous prospect for the existing semiconductor technology [1–3]. Several studies pertaining to the growth of self assembled In(Ga)As QDs directly on planar silicon substrate have been made over the past decade [1–4]. However, the heteroepitaxial growth of III/V QDs directly on flat silicon substrates has proven to be quite challenging due to the defects caused by dislocations and anti-phase domains, which originate from the large lattice and thermal expansion mismatch and polar/non-polar nature of III/V and Si systems [5–7]. These structural defects are closely related to carrier dynamics in the QDs and have severe influence on their optical quality. It has been proposed that these structural defects may be circumvented by realization of III/V QDs on pre-patterned substrates due to size effect of the patterned features [8]. For the large scale fabrication of single quantum light sources, tremendous progress in the growth of In(Ga)As QDs on pre-patterned GaAs substrates has been made [9–11]. Site-controlled In(Ga)As QDs with very narrow linewidth photoluminescence signal have been achieved both in inverted pyramidal [12–15] and circular nanoholes [16,17]. In recent years, some research efforts have also been made to realize the growth of III/V QDs on pre-patterned Si substrates using SiO_2 as a mask which show encouraging results [7,8,18]. Several lithographic techniques are in use for the pre-growth patterning of substrates, they include patterning of small holes with focused ion beam, scanning probe techniques and electron beam lithography [11]. However, the electron beam lithography is the most widely used technique to fabricate features in the sub-100 nm and in some cases even sub-10 nm range [19]. The details of the processing for the pre-growth patterning of the Si substrate with sub-100 nm holes have not been reported explicitly. In this contribution, we present the results of the optimized electron beam lithography and dry etching processes for the patterning of silicon substrates with sub-100 nm holes. The MBE growth of QDs on patterned Si surface with highly selective formation of localized dome like nanostructures in patterned holes with 1 μm period is also discussed.

2. Experimental details

Exactly oriented Si (100) substrates were used for patterning processes. The substrate was cleaned for 2 min each in acetone and isopropyl alcohol (IPA) and spin coated with positive tone electron beam resist polymethyl methacrylate (PMMA) to achieve a thickness of about 200 nm. The resist was exposed to define sub-100 nm holes by Raith e-line electron beam lithography (EBL) device in the form of single pixel dot exposure. After the exposure the resist was developed with standard 1:3 methyl isobutyl ketone (MIBK):IPA solution. The pattern was then transferred to the Si

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http://dx.doi.org/10.1016/j.mee.2012.02.020

substrate by an optimized dry etch process using an Oxford PlasmaLab System100 ICP:RIE machine. The resist was then removed by soaking the substrate in acetone for 5 min. The substrate was further cleaned in IPA at 80 °C for 10 min and in oxygen plasma asher for 30 min to remove any residual resist particles and carbon contamination left after the lithographic processing. Finally, the substrate was cleaned with HF:H_2O (1:2) solution for two minutes to remove the native oxide. The substrates were loaded into a Varian Gen II molecular beam epitaxy (MBE) system within 10 min of ex situ chemical cleaning. During the growth of GaAs/InGaAs/GaAs nanostructures, the growth rate of gallium was 0.75 ML/s and of indium 0.13 ML/s, respectively. The beam equivalent pressure (BEP) for gallium and indium were 2×10^{-7} Torr and 9×10^{-8} Torr, respectively, and the arsenic BEP throughout the growth was 5×10^{-6} Torr. The V/III ratio was adjusted to about 20 for all growth runs.

3. Results and discussion

3.1. Optimization of EBL exposure parameters

In order to achieve sub-100 nm holes with controlled diameter and shape on the Si substrate, the electron beam lithography process parameters for single pixel dot exposure were optimized. The dependence of minimum clearance dose was examined as a function of electron beam acceleration voltage as shown in Fig. 1a. The optimal acceleration voltage for the used resist thickness of 200 nm is around 10 kV for which the smallest clearance dose is needed. For acceleration voltages below 10 kV the penetration depth of electrons is too low to expose the whole resist with practical doses. For a given beam acceleration voltage the diameter of the patterned hole increases linearly with the exposure dose due to beam spreading caused by increased generation of secondary electrons and their scattering through the resist (Fig. 1b). The holes patterned with smaller exposure dose (10 fC) have well defined round shape (Fig. 1c) whereas those with high exposure dose (100 fC) have traces of carbon contamination due to the carbonization of PMMA resist [20]. Low exposure dose (10 fC) was thus selected for the patterning of nanoholes on Si.

3.2. Development of suitable ICP dry etching process

The nanoholes pattern was transferred after the PMMA development to the underlying Si substrate by an ICP dry etching process. A highly anisotropic dry etching process based on SF_6 and CHF_3 gases was developed and optimized [21]. The dependence of Si etch rate, PMMA erosion rate and DC bias on the ICP power is depicted in the plots of Fig. 2a and b. These plots show that silicon etch rate increases linearly with the increasing ICP power due to the enhancement of the density of the F* etching species [22]. The DC bias rapidly increases when the ICP power is increased from 600 W to 800 W (Fig. 2b) after which the increment is less prominent, but the onset of the high PMMA erosion rate starts at ICP power of 800 W and strongly increases up to 1200 W. From this we conclude that enhanced erosion of PMMA from 800 W to 1200 W is mainly caused by ion bombarding due to the increased ion density rather than the ion energy, which is determined by the DC bias of the process. The selectivity of Si:PMMA = 2:1 is low but sufficient to etch nanoholes with a depth of few tens of a nm for the pre-patterned substrates. The sidewall profiles using optimized recipe for a 2 μm wide trench and a sub-100 nm nanohole have been shown in Fig. 2c and d respectively. The increasing sidewall tapering for nanohole can be attributed to an overpassivation effect for sub-100 nm features.

3.3. Characterization of pre-patterned Si substrates

Using the optimized electron beam lithography and dry etching recipe described in Sections 3.1 and 3.2, respectively, the Si substrates were patterned with square lattices of sub-100 nm holes with various periods ranging from 1 μm down to 200 nm. Fig. 3a shows the SEM profile of the patterned Si substrate for holes with 1 μm spacing. The surface morphology and the depth of the patterned holes were investigated by atomic force microscopy

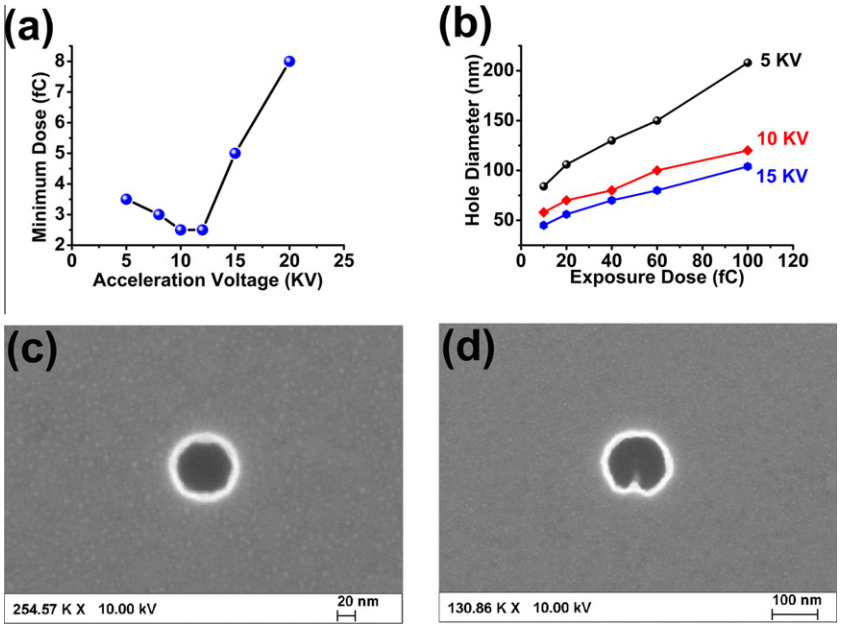

Fig. 1. (a) The minimum clearance dose dependence on electron beam acceleration voltage and (b) the variation of the diameter of the patterned hole with beam acceleration voltage. (c) The SEM profile of patterned hole with an exposure dose of 10 fC per single pixel dot, the diameter is about 60 nm and (d) with an exposure dose of 100 fC per single pixel dot, the diameter is around 120 nm.