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Nanostructured silicon for Ge nanoheteroepitaxy

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ABSTRACT

A fabrication process for Si nanopillars (NPs) as template for the Ge nanoheteroepitaxy (NHE) was developed. The NHE concept suggests that by fabricating three-dimensional free standing NP, the NP can be elastically deformed by deposited heteroepitaxial material on the top due to lattice mismatch strain. To enable the elastic deformation, small diameter NPs are required with a specific height. A fabrication process was developed to create Si NPs with <100 nm width and >100 nm height. The top of Si NPs must be opened for selective Ge growth, while the sidewall and bottom surface must be covered by SiO_2. Spectroscopic ellipsometry was used to control Si NPs before selective Ge epitaxial overgrowth. The process was optimized based on transmission electron microscopy (TEM) and X-ray diffraction investigations. Ge on top of NPs is fully relaxed. The relaxation occurs however not elastically but plastically by misfit dislocation nucleation at the Ge/Si interface due to SiO_2 passivation of the sidewall. The possible approaches to enable elastic deformation of Si NPs are to reduce the SiO_2 thickness of the sidewall and lateral dimension of NPs. The Ge of high crystallinity grown on top of the NPs only is indicating that the developed technology guarantees a clean top Si surfaces and a sufficient SiO_2 protection of the rest of the structure. No threading dislocations are observed by TEM. This shows that the small lateral dimension of the seed area allows the TDs to glided out to the surfaces with high probability.

1. Introduction

The integration of Ge heterostructures on Si (0 0 1) is of greatest interest for new applications in micro and optoelectronics as e.g. high mobility channel CMOS technologies [1], optical data communication [2] or as mediator material to achieve the manufacturing of III–V/Si hybrid devices [3]. The quality of Ge, i.e. low defect density of threading dislocations (TDs) is of high importance for any applications [4]. The key problem to achieve Ge thin film heterostructures suitable for device applications is the strong lattice mismatch between Ge and Si of about 4.2%.

Different approaches are reported [5–15] to deposit Ge layers on blanket Si wafers with low threading dislocation density (TDD). One way is to introduce thick graded SiGe buffer layer [5], another is the direct deposition of Ge on Si with annealing steps during and after the Ge layer growth [6–8]. TDD as low as 7×10^5 cm^{-2} are reported for 4.7 μm thick Ge layer with low level of surface roughness (RMS ~0.45 nm) [9]. However for all cases, the huge intra-chip topology due to thick Ge growth causes interconnect problems between optoelectronics and CMOS devices. Recently, the direct Ge deposition and etching technique which succeeded to a substantially reducing of Ge thickness (down to ~1 μm) without degrading TDD (achieving $< 1 \times 10^7$ cm^{-2}) were reported [10]. Further reduction of Ge thickness is preferred for the Ge device integration into CMOS. Other method to deposit low TDD Ge with limited thickness is to use the high aspect ratio window to trap the TDs [13–15]. By this technique, the TDD of 10^6–10^7 cm^{-2} is achieved [15].

A very promising method for further reduction the Ge thickness is the nanoheteroepitaxy (NHE) approach, which is reported by Zubia et al. [16,17]. In this work, NHE was performed for selective Ge nanostructure growth on free standing Si nanopillars (NP). The biggest potential of this technique is the capability of the elastic deformation of the NP known as the compliant substrate effect. This work is concentrated on the fabrication process for NPs with $\leqslant$100 nm width and >100 nm height with clean top Si surface and passivation of the rest of the structure (sidewall, bottom surface) by SiO_2 as template for Ge heteroepitaxy. However the critical point for new defect generation in all techniques with laterally limited growth is the coalescence process during which stacking faults etc. might be formed.

2. Experimental

The NP structuring scenario including the selective Ge heteroepitaxy strategy is illustrated in Fig. 1. The lithography was

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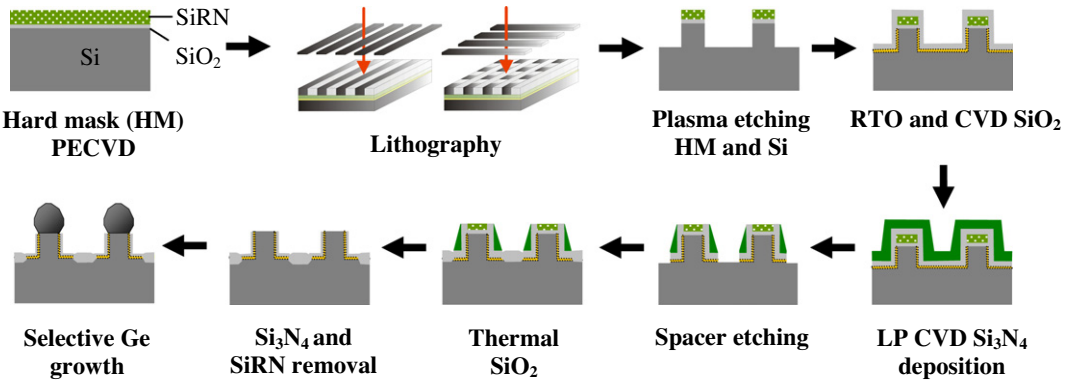

Fig. 1. Schematic illustration of the fabricated NPs and Ge epitaxial growth process.

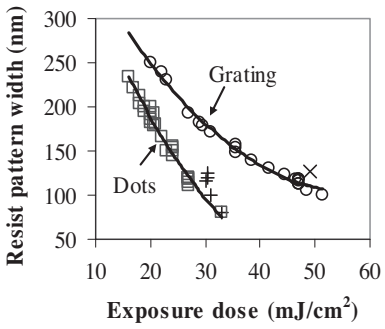

Fig. 2. Resist pattern dimension versus the exposure dose (□, ○ – pitch = 360 nm, +, × – pitch = 260 nm) for dots performed by crossed double exposure grating and single exposure grating.

carried out by using KrF (248 nm) deep-UV Nikon Scanner S207 with crossed double exposure grating structures for dot structures and with a single exposure for grating patterns. The exposure was done with the numerical aperture of 0.82 and coherence parameter of 0.9 and using the 335 nm thick chemical amplified positive resist UV2000 (Dow). The dimension of the dots and the gratings are adjusted by changing exposure dose of lithography process. The SiO_2 sidewalls, as one of the important parameter for NHE, is formed by 5 nm rapid thermal oxidation (RTO) followed by low pressure chemical vapor deposition (LPCVD) using tetraethoxysilan (TEOS) varied to get final thickness from 10 to 40 nm. After the native SiO_2 removal on the top of NPs by HF last clean, the Ge growth is performed using single wafer reduced pressure chemical deposition (RPCVD) with N_2–GeH_4 gas mixture at 300 °C. After that the wafer is heated up to 550 °C in H_2 and the Ge growth is continued with a H_2–GeH_4 gas mixture. The special process conditions are reported elsewhere [10].

The capability of spectroscopic ellipsometry (SE) as a noninvasive measurement method for nanopatterned surfaces was used for in line process control of the Si nanostructures. The rigorous coupled wave analysis (RCWA) was used to fit the ellipsometric parameters ($\tan\psi$ and $\cos\Delta$). For the simulations, the UNIGIT software was applied [18]. The Si NPs height and width as well as the sidewall and the bottom SiO_2 thickness of the grating were used as the floating parameters. Scanning electron microscopy (SEM) is used for the process control, transmission electron microscopy (TEM) is used for evaluation of dislocations and X-ray diffraction (XRD) is used for strain analysis with the goal of process optimization.

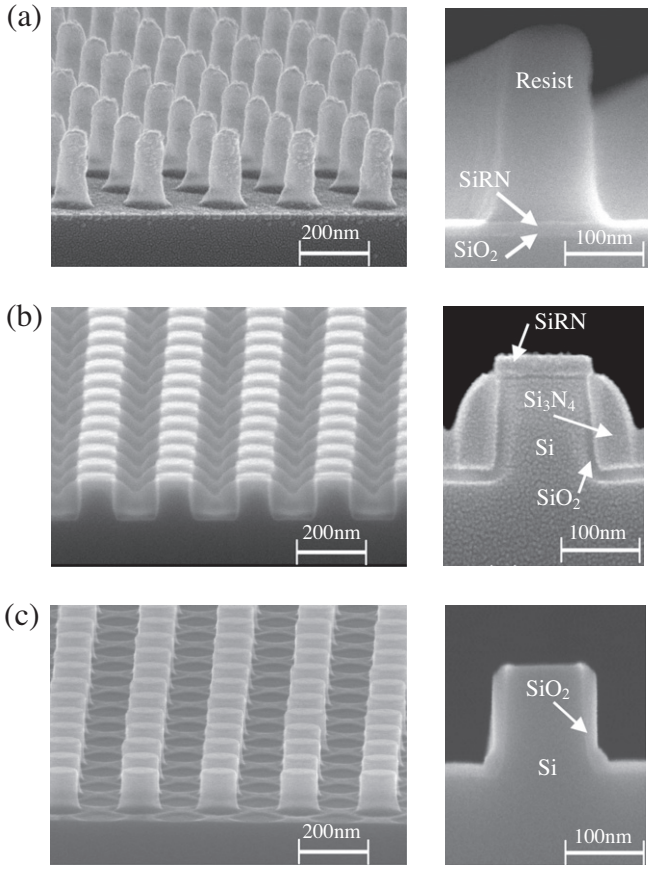

Fig. 3. SEM images after (a) lithography pattern, (b) spacer plasma etching process, and (c) Si_3N_4 and HM removal and HF last clean.

3. Results and discussion

In order to fabricate the targeted dimension of NPs, the required exposure dose is expected to differ from the conventional single exposure lithography process. Therefore the impact of the exposure dose on the resist width for single exposure (gratings) and double exposure (dots) are investigated (Fig. 2). The exposure dose is varied from 20 to 50 mJ/cm^2. It was found that the exposure dose required a factor of about 1.45 for the grating patterning to achieve equal dimension. The optimized process steps start with minimal resist dots of 115 nm width shown in Fig. 3a. SiO_2 and Si rich nitride (SiRN) are used as an anti-reflective coating for the lithography. The SiRN was adjusted for optimized antireflection [19]. Both