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Regular Article

Impact of diamond seeding on the microstructural properties and thermal stability of GaN-on-diamond wafers for high-power electronic devices

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ABSTRACT

The impact of seeding of the diamond growth on the microstructural properties of GaN-on-diamond wafers was studied using in situ focused ion beam cross-sectioning and scanning electron microscopy imaging. Microstructural studies revealed that the seeding conditions are a critical parameter to obtain an optimal material, allowing the manufacture of GaN-on-diamond wafers with no microscopic defects and with structural stability under thermal annealing at 825 °C. The use of the right seeding conditions also results in homogeneous thermal properties across four inch GaN-on-diamond wafers, which is of critical importance for their use for ultra-high power microwave electronic devices.

AlGaN/GaN-on-diamond microwave devices have demonstrated at least three times higher power density than devices grown on SiC substrates [1,2]. Since GaN-on-diamond substrates were first demonstrated [3], various groups have shown that diamond as substrate permits a more compact device design, enabling reduced gate finger spacing compared to devices on SiC substrates [1,4,5]. This allows for a dramatic shrinkage in monolithic microwave integrated circuits (MMIC) or power amplifier (PA) size and hence an increase in their efficiency through the removal of lossy combining networks. All this is due to the thermal conductivity of diamond, as high as 2000 W/mK at 300 K compared to 450 W/mK for SiC, which improves the waste heat extraction from the active device area [6]. The AlGaN/GaN layers in AlGaN/GaN-on-diamond devices typically originate from a qualified epitaxy, for example grown on Si substrates. Diamond growth or wafer-bonding is then used to replace the original substrate [1,7,8]. To enable large-scale integration (>four inch wafers), the diamond is grown on the N-face of the (Al)GaN epitaxial layers, using a thin dielectric layer to allow the seeding of the diamond onto the GaN [1]. This makes the GaN/diamond interface the critical region to be optimized in order to maximize the performance of devices. In recent years significant improvements in the thermal transport properties of the GaN/diamond interface have been achieved; for example the optimization of the GaN/diamond interfacial dielectric layer and the improved thermal properties of diamond near its nucleation site at the GaN/diamond interface [9–11]. As a consequence of these advances in understanding, it is now considered possible to achieve the best device characteristics by further optimizing the thermal transport at and/or near the GaN/diamond interface. This can be realized by adjusting the grain size of the diamond crystallites to be as large as possible near the nucleation region for maximized thermal conductivity [11] while the dielectric layer used to seed the diamond is kept as thin as possible to minimize its thermal resistance [9]. A straightforward strategy to adjust the grain size, targeted in this work, which has not been explored previously, is to modify the size of the diamond seeds used to grow the diamond underneath the GaN epitaxial layers. However, this strategy might influence the integrity of the GaN/diamond interface by promoting the formation of defects and voids which may impact the thermal and mechanical properties of the interface which is unknown. We emphasize that the mechanical properties are extremely crucial for the reliability of the material [12] since this interface is prone to be affected by the significant coefficient of thermal lattice expansion (CTE) mismatch between the diamond and the GaN. In this letter, the implication of different diamond seeding strategies, namely using larger and smaller seeding nanoparticles, on the ultimate microstructure, thermal properties of GaN-on-diamond wafers and its reliability are addressed. We demonstrate that GaN-on-diamond materials can be free from microscopic defects and have good homogenous thermal performance, however, this can only be achieved if an appropriate diamond seeding approach is used.

For the GaN-on-diamond wafers studied, AlGaN/GaN heterostructures grown on Si substrates by metal-organic chemical vapor deposition (MOCVD) were used as the starting material. A SiN dielectric layer

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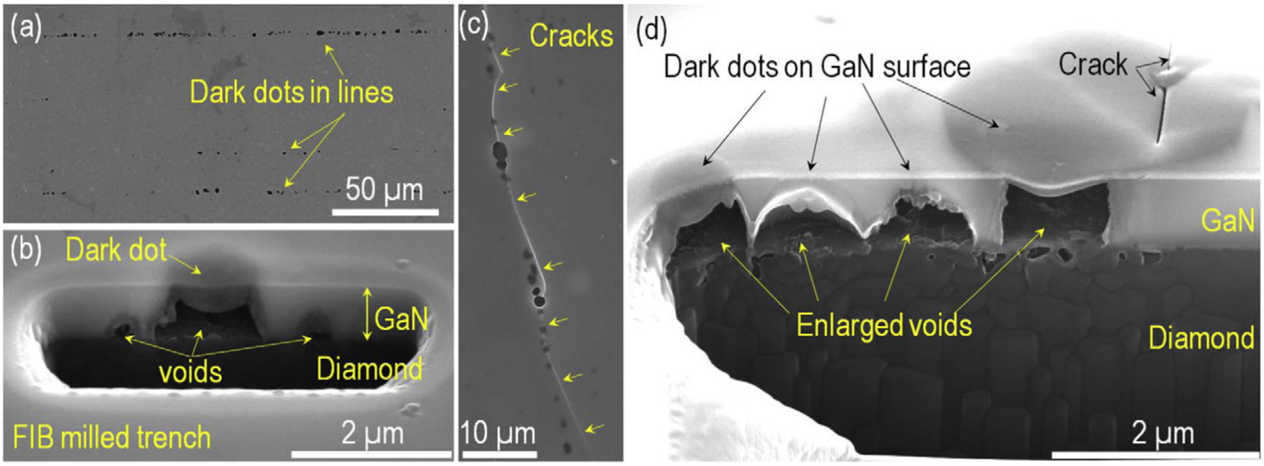

Fig. 1. Scanning electron microscope (SEM) images of as-manufactured GaN-on-diamond grown with 100 nm diamond seeds showing (a) lines of dark dots on the surface of GaN denoted as type A defects; (b) voids at the GaN/diamond interface underneath a typical dark dot in (a); (c) cracks are formed on the surface of GaN along the dark dots after 825 °C annealing, and (d) the interfacial voids are more pronounced after annealing.

was deposited on top of the structure to protect the device layer surface. The Si substrate and the AlGaN strain relief layer were then removed; a post grind and lap clean step was used to ensure that there is no residual AlGaN prior to the deposition of a 30 nm thin amorphous dielectric layer by low-pressure CVD for diamond seeding. As diamond growth is in a harsh environment with atomic hydrogen and high temperatures, the dielectric layer protects the GaN during this process. Diamond nanoparticles with two different average sizes, 30 nm and 100 nm diameter, were used for the seeding of the diamond growth, respectively. For the 30 nm seeding, seeding density was better than 1×10^{11} cm^{-2}; for the 100 nm seeding, the density was about 1×10^{10} cm^{-2}. In both cases, a 100 μm thick diamond layer was grown using microwave (MW) plasma CVD. Further details on the GaN-on-diamond structure and sample fabrication can be found in Ref. [11]. As-manufactured samples, and samples annealed at 825 °C in nitrogen (temperature ramped up in 90 s, hold for 20 s, then cool down to room temperature over a period of 60 s) were studied since this is an annealing condition typically used during the processing of devices for ohmic contact formation.

Characterization of the wafers was undertaken in a FEI Helio NanoLab 600i Dualbeam workstation. In particular, trenches were etched into the wafer by focused Ga^{+} beam at a number of locations to create cross-sections of the GaN-on-diamond structure; a voltage of 30 kV and current of 6.5 nA was used, and this was followed by a final cleaning step with a much lower current, 48 pA. Cross-sections of the GaN-on-diamond structure were then reviewed and the microstructure characteristics evaluated by scanning electron microscope (SEM) imaging. All these cross-sectional images were taken at a stage tilt of 52° to allow the in situ observation of the surface features as well as the cross-sections. In addition, the thermal properties of the GaN-on-diamond wafers were mapped by transient thermoreflectance and correlated to local microstructural features. A heating pulse from a 355 nm frequency-tripled Nd:YAG laser (3.49 eV, i.e., above GaN bandgap) was absorbed into the GaN, with a pulse duration of 10 ns inducing a surface temperature rise. The resulting change in surface reflectance was monitored by a continuous wave (CW), 532 nm frequency-doubled Nd:YAG laser to track this temperature rise. From this the thermal boundary resistance (TBR_{eff}) of the GaN/diamond interface could be determined. Heating and probe laser spot sizes were 60 μm and 2 μm respectively. Further details on this technique can be found in Ref. [13].

In general, for specimens grown with 100 nm diamond seeds, two types of defects were observed; denoted in the following as Type A and Type B. Type A, as shown in Fig. 1, appear as dark dots on the surface of the as-manufactured material under SEM imaging. These dots tend to follow straight lines and some are randomly distributed, Fig. 1a. Focused ion beam milling was used to cut trenches across these dark dots to reveal the cross-sectional features. It was found that these dark dots correspond to voids at the GaN/diamond interface, Fig. 1b. Some of these voids are of a size equivalent to the thickness of the full GaN layer (900 nm in this case), i.e. penetrate to the surface (through-holes), while others are much smaller and remain concentrated at the GaN/diamond interface. After annealing at 825 °C, however, a larger number of these dark dots was found on the surface; cracks also formed, Fig. 1c, usually aligned with a line of dark dots, but they can deviate at defined angles. FIB cross-sectioning on these annealed samples indicates that with annealing (Fig. 1d) local debonding occurred; the interfacial voids have grown in size. In addition to an interfacial GaN/diamond debonding at the sites of the voids, other factors such as residual stresses in the GaN layer may have contributed to the propagation of cracks along cleavage planes of the GaN. Small voids also formed inside the diamond near the interface at these locations. Type B defects are nanosized pinholes in the dielectric layer at the GaN/diamond interface in the as-manufactured material, Fig. 2a. In some areas, cavities along the interface form with 'teeth-like' features between GaN and the diamond layer, Fig. 2b. These features are observed in both as-manufactured samples and after annealing.

As the dark dots (Type A defects) are mostly arranged in lines, this strongly suggests a mechanical abrasion process damaging the dielectric seed layer when the 100 nm diamond seeds are deposited. When the material structure is subsequently exposed to the diamond growth

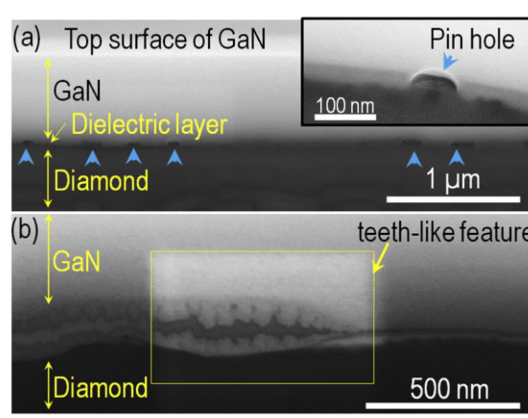

Fig. 2. SEM images showing FIB milled cross-sections of (a) pinholes at the dielectric layer between the GaN and the diamond in as-manufactured material grown with 100 nm diamond seeds (type B defects, marked by arrows; insert is a picture of the pinholes at a larger magnification) and (b) cavity at GaN/diamond interface with teeth-like features.