Microelectronic Engineering 89 (2012) 15–18

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Reliability characteristics of metal-oxide-semiconductor capacitors with 0.72 nm equivalent-oxide-thickness LaO/HfO_2 stacked gate dielectrics

Chuan-Hsi Liu [a,*], Hung-Wen Hsu [b], Hung-Wen Chen [b,*], Pi-Chun Juan [c], Mu-Chun Wang [d], Chin-Po Cheng [a], Heng-Sheng Huang [b]

[a] Department of Mechatronic Technology, National Taiwan Normal University, No. 162, Sec. 1, He-Ping E. Rd., Taipei 106, Taiwan
[b] Institute of Mechatronic Engineering, National Taipei University of Technology, No. 1, Sec. 3, Chung-Hsiao E. Rd., Taipei 106, Taiwan
[c] Department of Materials Engineering, Ming Chi University of Technology, No. 84, Gungjuan Rd., Taishan, Taipei 243, Taiwan
[d] Department and Institute of Electronic Engineering, Minghsin University of Science and Technology, No. 1, Xinxing Rd., Xin Feng, Hsinchu 304, Taiwan

ARTICLE INFO

Article history:
Available online 19 May 2011

Keywords:
High-*k* dielectric
La-incorporated HfO_2
TDDB reliability

ABSTRACT

La-incorporated HfO_2 could improve the thermal stability and interface trap quality. Laminated structures with different doping positions and thicknesses were fabricated by RF magnetron co-sputtering method. The physical and electrical properties of HfO_2/HfLaO/p-Si and HfLaO/HfO_2/p-Si structures after 850 °C postannealing were analyzed. And the time dependent dielectric breakdown (TDDB) characteristics were also analyzed for metal-oxide-semiconductor (MOS) capacitors with atomic-layer-deposited (ALD) HfLaO gate dielectrics. For TDDB characteristics, the Weibull slopes were independent of stress voltages and capacitor areas, but they were dependent on the stress temperatures. The electric-field acceleration parameter (γ) is about 4.3–4.5 MV/cm. The maximum voltage (V_g) for 10-year TDDB lifetime under 85 °C operation is V_g = 2.03 V, or equivalently 6.1 MV/cm.

1. Introduction

Hafnium dioxide (HfO_2) gate dielectric has been considered one of the most promising candidates for current and future gate dielectric applications [1,2]. Nevertheless, HfO_2 gate dielectrics have encountered the following two major issues: (1) low crystallization temperature and (2) high threshold voltage (V_T) caused by Fermi-level pinning or oxygen vacancy [3,4]. Researchers have introduced Si, Al, N, or Ta into HfO_2 gate dielectrics to increase the thermal stability and solve Fermi-level pinning issue [5–9]. Although these efforts can improve crystallization temperature and obtain low V_T with low effective work function ($\Phi_{m,eff}$), the dielectric constants as well as the barrier heights at gate/dielectric and dielectric/substrate interfaces decrease significantly in comparison with pure HfO_2 [10]. More recently, rare earth metal lanthanum (La) incorporation into HfO_2 has been successfully demonstrated to achieve desired device characteristics with adjustable V_T, increased crystallization temperature without degradation of dielectric constant, and improved positive-bias-temperature-instability (PBTI) reliability [11,12]. Though it is well accepted that time-dependent dielectric breakdown (TDDB) is one major concern in advanced technology, it has not yet been fully understood for HfO_2-based high-κ dielectrics, especially for La-incorporated HfO_2 gate dielectrics.

In this work, the pilot study was first done by using MOS capacitors with the HfO_2 dielectrics incorporating different La doping positions and concentrations. After the analysis of the pilot study, advanced MOS capacitors with atomic-layer-deposited (ALD) LaO/HfO_2 stacked gate dielectrics were also fabricated. The physical and electrical properties of pilot-study devices were analyzed. The TDDB characteristics of the advanced devices with LaO/HfO_2 stacked dielectrics were investigated in this article.

2. Experiments

In this study, we fabricated two kinds of devices, pilot-study devices and advanced devices. For the pilot-study devices, the starting substrates used the *p*-type (1 0 0) orientation, 4-inch diameter silicon wafers. High-k hafnium lanthanum oxides (HfLaO) were co-deposited by RF magnetron sputtering at room temperature. The thickness of each laminated structure was designed to be 7 nm. A post-deposition annealing (PDA) was performed in pure N_2 at 850 °C for 30 s. Then aluminum was used as the top electrode.

The MOS capacitors of advanced devices were fabricated on 12-inch *p*-type (1 0 0) Si wafers. After the standard cleaning procedures, 2-nm ALD HfO_2 thin film was deposited on *p*-Si substrate, followed by 1-nm ALD LaO thin film. Then, a 10-nm TaC metal gate was deposited by physical vapor deposition (PVD) as the gate electrode and capped by poly-Si. Finally, a post-metal-anneal was employed at 420 °C in forming gas for 30 min. The *C*–*V* curve was measured and the EOT is 0.72 nm [13]. The various areas of MOS

* Corresponding authors. Tel.: +886 2 77343515; fax: +886 2 23583074.
E-mail addresses: liuch@ntnu.edu.tw (C.-H. Liu), iou1166@yahoo.com.tw (H.-W. Chen).

0167-9317/$ - see front matter © 2011 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2011.04.009

capacitors range from 3.1×10^{-6} to 1.0×10^{-4} cm^2. All current–voltage (I–V) characteristics were measured through Agilent 4156C parameter analyzer.

3. Results and discussion

3.1. Physical and electrical properties

Fig. 1 shows the X-ray diffraction (XRD) patterns of HfO_2 (7 nm)/p-Si, HfLaO (4 nm)/HfO_2 (3 nm)/p-Si and HfO_2 (4 nm)/HfLaO (3 nm)/p-Si structure. The crystalline peak of HfO_2 (7 nm)/Si structure is observed around $2\theta = 30°$, but there is no crystalline phase observed in other two structures. It means that the addition of La could improve the thermal stability for annealing temperature up to 850 °C. It may be because La_2O_3 has a higher film crystallization temperature in comparison with HfO_2 [14]. Fig. 2 shows the XRD patterns with different incident angles of 0.3, 0.5, and 1° for (a) HfO_2 (6 nm)/HfLaO(1 nm)/Si and (b) HfLaO (6 nm)/HfO_2 (1 nm)/Si. From Fig. 2(a), a peak observed around $2\theta = 30°$ is the crystallization phase of the dielectrics, indicating that the film is prone to crystallization for the conditions where HfLaO was first deposited on the silicon substrate, and moreover the concentration of lanthanum has significant effect on the crystallization temperature of the films [11]. Shown in Fig. 2(b), there is no peak observed in the HfLaO (6 nm)/HfO_2 (1 nm)/p-Si structure around $2\theta = 30°$. Therefore it is clear that the structure in which HfO_2 was first deposited on the silicon has better thermal stability.

The leakage current density versus voltage (J–V) properties of Al/HfLaO (x nm)/HfO_2 ($7 - x$ nm)/Si and Al/HfO_2 (x nm)/HfLaO ($7 - x$ nm)/Si with $x = 4$ and 6 were compared, as shown in Fig. 3. From this figure we can see the structure where HfLaO was first deposited on the silicon substrate has larger leakage current for $x = 4$ or 6. For the dielectrics with HfLaO in contact with the silicon substrate, the crystallization temperature decreases as the concentration of La decreases [11]. The gate leakage current increases when the dielectric is crystallized. Because a smaller leakage current density was desired [15], the structures with HfO_2 in contact with the silicon substrate were therefore chosen for the advanced MOS capacitors.

3.2. TDDB characteristics

The gate leakage current versus stress time (I_g–t) characteristics of the MOS capacitors with various areas are shown in Fig. 4, where time-to-breakdown (T_{BD}) is defined as hard breakdown (HBD) occurs. Fig. 5 shows the area-scaled Weibull distributions of different capacitor areas (A_x) normalized to those of 1.0×10^{-5} cm^2 samples (A_{norm}) by multiplying $\ln(A_x/A_{norm})$ [16]. The normalized Weibull distributions of two different capacitor areas are matched to a single line, meaning that the breakdown is intrinsic and it can be explained by percolation model [17]. Fig. 6 shows the TDDB Weibull distributions of different capacitor areas under various

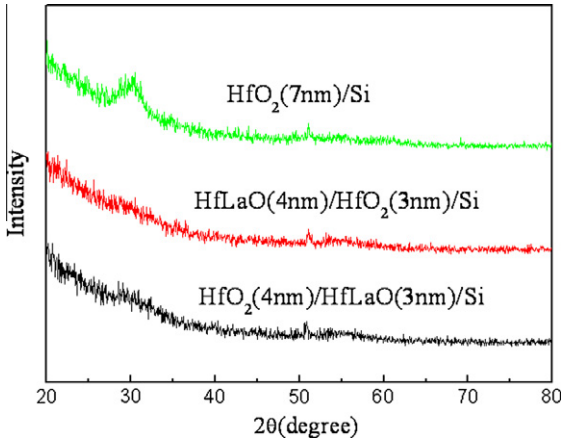

Fig. 1. X-ray diffraction patterns of HfO_2 (7 nm)/Si, HfLaO (4 nm)/HfO_2 (3 nm)/Si, and HfO_2 (4 nm)/HfLaO (3 nm)/Si structures at postannealing temperature of 850 °C. The incident angle is 1°.

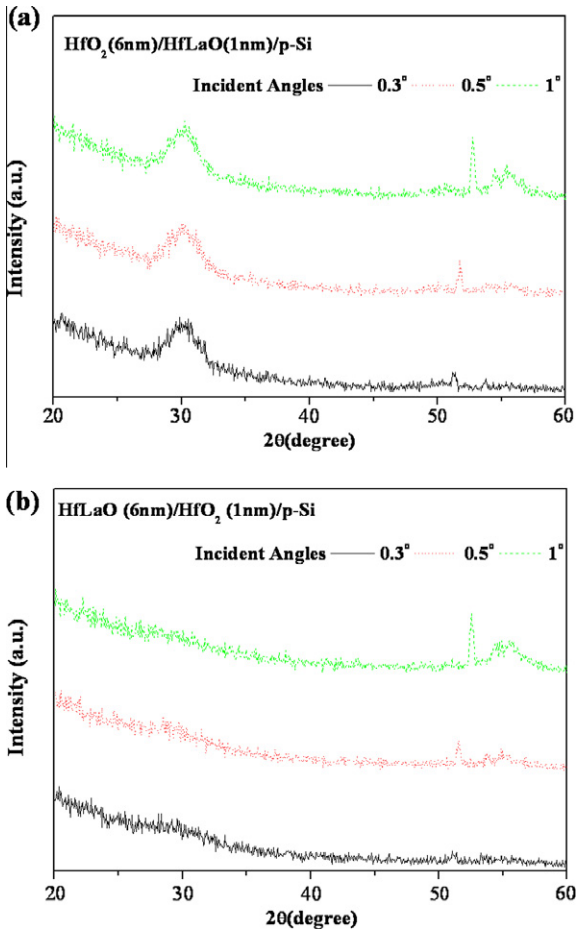

Fig. 2. X-ray diffraction patterns of (a) HfO_2 (6 nm)/HfLaO(1 nm)/Si, and (b) HfLaO (6 nm)/HfO_2 (1 nm)/Si with different incident angles at postannealing temperature of 850 °C.

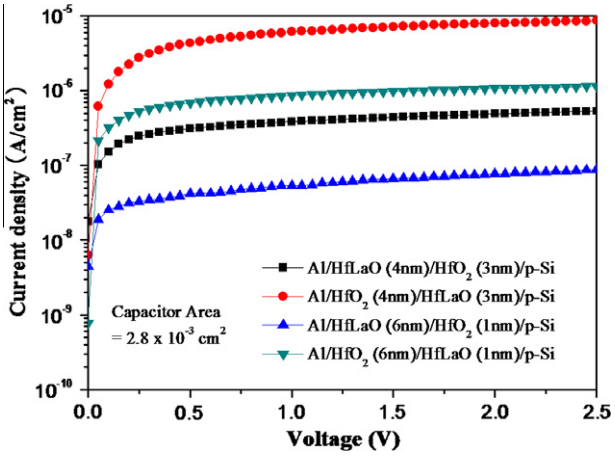

Fig. 3. Leakage current density versus voltage properties of Al/HfLaO(x)/$HfO_2(7 - x)$/Si and Al/$HfO_2(x)$/HfLaO($7 - x$)/Si, where $x = 4$ or 6 nm.