Microelectronic Engineering 89 (2012) 37–41

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Degradation of n-channel low temperature poly-Si TFTs dynamically stressed in OFF region with positive drain bias

Han-Wen Liu *, Si-Ming Chiou, Han-Ching Ho, Fang-Hsing Wang

Department of Electrical Engineering and Institute of Electrical Engineering, and Graduate Institute of Optoelectronic Engineering, National Chung Hsing University, Taichung 402, Taiwan, ROC

ARTICLE INFO

Article history:
Available online 9 January 2011

Keywords:
Low temperature poly-Si
Thin-film transistors
AC stress
Sampling current
Reliability

ABSTRACT

The degradation characteristics of n-channel low temperature poly-Si thin film transistors (LTPS TFTs), which are alternately stressed in OFF region with drain positively biased and source grounded, are investigated. In this research, rectangular pulse signals, dynamically changing from −18 to 0 V with varied parameters such as rising time, falling time, and frequency, are applied to the gate terminal, and the drain is simultaneously biased at +5 V to stress the LTPS TFTs and examined the deterioration. It is observed that the degradation strongly depends on the frequency and rising time rather than the falling time of AC signals. As the gate voltage transitionally changes in the rising period, the accumulated holes should be swept out and flow into the source terminal, resulting from the drain with positively biased and the floating body structure of TFTs. A degradation model of the parasitic BJT, based on the flowing direction of a sampling current I_d, is proposed to explain the degradation mechanism of LTPS TFTs, and demonstrated by two electrical measurements, C–V curves and saturated forward and reverse I_d–V_g transfer curves.

1. Introduction

Low temperature poly-Si thin-film transistors (LTPS TFTs) have attracted considerably much interest in the flat panel displays (FPDs). Due to the much higher free carriers' mobility of the LTPS TFTs, about 100 times larger than that of amorphous silicon (a-Si) TFTs, they can be employed in not only the in-pixel switches but also in the peripheral driving circuits for the active matrix displays. The system on panel (SOP) concept would be realized as the driving capability of LTPS TFTs further improves. Although the improvement of mobility is the most important subject in the high performance display applications, the instability evaluation of LTPS TFTs is as well as the essential theme for the reliability promotion of driving circuits. The previous reports focus on investigating the degradation of the poly-Si TFTs under AC stress with the applied gate voltages allowing the TFTs to change from the OFF state to the ON state [1–4], or the ON state only [5–7]. However, the gate terminals of poly-Si TFTs in the driving circuits are imposed with the high frequency AC signals and may be toggled into the OFF state with data in the drain or source terminals. Therefore, the instability of LTPS TFTs dynamically operated in the OFF state with the drain positively biased and source grounded need to be investigated in detail. As yet, there are very few researches focusing on this issue [4,8]. It has been reported that degradation by pulse swing for the ON region was very small but large for the OFF region [4]. However, the degradation mechanism for the AC stress in OFF region, which is dependent on falling time (T_f) or rising time (T_r) of the pulse signals, is not examined. In addition, the gated p–i–n poly-Si TFTs have been reported to investigate the degradation mechanism of TFTs dynamically operated in OFF region [8]. However, the gated p–i–n poly-Si TFTs are not the real device's structure in the driving circuits.

In this study, we directly employ the conventional n-channel LTPS TFTs with a lightly doped drain (LDD) structure to investigate the reliability of devices stressed in the OFF state with the drain positively biased and source grounded. A degradation model of the parasitic BJT [9] is proposed to explain the deterioration of LTPS TFTs alternatively operated in the OFF state with the drain positively biased and source grounded. Coinciding with the previous researches under AC stress, the degradation of LTPS TFTs is also accelerated by the transient stress. On the contrary, the T_r rather than T_f of the pulse signals imposed on the gate terminal is the dominant transient stress for the LTPS TFTs dynamically stressed in the OFF state with the drain positively biased and source grounded.

2. Experimental procedure

The planar and top-gated n-channel LTPS TFTs with LDD structure are used in this study. The channel width and length are 20 μm and 5 μm, respectively, and the length of LDD is 1.5 μm.

* Corresponding author. Tel.: +886 4 22851549.
E-mail address: hwliu@dragon.nchu.edu.tw (H.-W. Liu).

0167-9317/$ - see front matter © 2011 Elsevier B.V. All rights reserved.
doi:10.1016/j.mee.2011.01.021

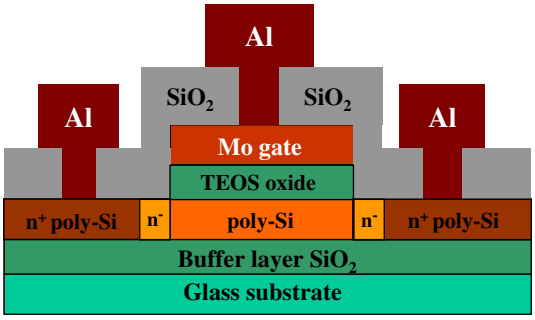

Fig. 1. Schematic cross-sectional diagram of low temperature poly-Si TFTs with LDD structure.

The fabricating procedures of LTPS TFTs are described as follows. First, the buffer oxide and 50 nm-thick hydrogenated amorphous silicon (a-Si:H) thin films are deposited by the plasma-enhanced chemical vapor deposition (PECVD) on the glass substrate. After the dehydrogenation process, the XeCl excimer pulse laser with 308 nm wavelength and 400 mJ/cm^2 energy density is adopted to transfer the a-Si film to poly-Si. After the definition of active region, the 100 nm-thick tetraethoxysilane (TEOS) SiO_2 is deposited by PECVD as the gate oxide. The metal gate of Mo is formed by the sputtering and patterning process. Next, the LDD is constructed by $^{31}P^+$ self-aligned implantation with the dosage 2×10^{13} cm^{-2}, and the n^+ source and drain regions are done by $^{31}P^+$ implantation with the dosage 5×10^{15} cm^{-2} and separate mask. Then the 500 nm-thick passivation SiO_2 is deposited by PECVD. Subsequently, the samples are annealed at 600 °C in N_2 for 24 h to activate the dopants. Hydrogenation process is performed to improve the electrical property of the LTPS TFTs. Finally, contact holes formation, metallization, gate, drain, and source metal pads are defined to complete the fabrication processes. The schematic cross-sectional diagram of LTPS TFTs with LDD structure is illustrated in Fig. 1.

The pulse trains are applied to the gate terminal and the drain is simultaneously biased with +5 V as the AC stress, and the source grounded. The alternate pulses with −18 to 0 V, 50% duty ratio, and frequencies of 10 kHz–10 MHz are used in this study. Because the threshold voltage (V_{th}) of n-channel LTPS TFTs is about 1.5 V, these devices will always stay in the OFF state as above voltage pulses imposed on the gate terminal. The T_r and T_f are varied from 5 to 200 ns, individually. The definition of on-current (I_{on}) is the drain current (I_d) corresponding to the V_g = +10 V and V_d = +0.1 V. The degradation of I_{on} is defined as $\Delta I_{on}/I_{on,0}$, where $I_{on,0}$ is the initial I_{on} and ΔI_{on} is the difference between $I_{on,stress}$ (I_{on} after stress) and $I_{on,0}$. Furthermore, the transconductance (G_m) is derived by differentiating the I_d with respect to the V_g as the LTPS TFTs operated in the linear region, i.e. I_d–V_g transfer curve with V_d = +0.1 V. We examine the degradation of maximum transconductance ($G_{m,max}$) by the $\Delta G_{m,max}/G_{m,max,0}$, where $G_{m,max,0}$ is the initial $G_{m,max}$ and $\Delta G_{m,max}$ is the difference between $G_{m,max,stress}$ ($G_{m,max}$ after stress) and $G_{m,max,0}$.

3. Results and discussion

The dependence of I_{on} and $G_{m,max}$ degradation of LTPS TFTs on the stress time are shown in Figs. 2a and 3a, respectively. The stress conditions are V_g = −18 to 0 V, V_d = +5 V, V_s grounded and $T_r = T_f$ = 5 ns under several frequencies. It is observed that as the pulse frequency increases, the degradation of LTPS TFTs becomes more severe, which is similar to the previous reports with the pulse voltages ranging from the OFF state to the ON state [1–4], or the ON state only [5–7]. Therefore, the frequency-related degradation exhibits that the deterioration mainly occurs in the transitional time. To further study the relationships between the pulse frequency of AC stress and the degradation, the dependence of I_{on} and $G_{m,max}$ degradation on the pulse frequency and stress time are re-plotted as the dependence on pulse repetition numbers, the product of pulse frequency and stress time, as shown in Figs. 2b and 3b, respectively. No relationship between the applied pulse frequency and the degradation trends of I_{on} and $G_{m,max}$, is observed and all of the lines follow the universal curve as a function of repetition numbers. The larger the repetition numbers are, the more severe LTPS TFTs deterioration is. These results clearly describe that repetitions of the imposed gate voltage from −18 to 0 V (rising period) or from 0 to −18 V (falling period) would accelerate the device's degradation. There is slight difference in the universal curves of Figs. 2b and 3b, resulting from the influence of V_{th} shift which increases about 0.2–0.9 V after 2000 s stress under the pulse frequencies ranging from 10 kHz to 10 MHz. It is known that the degradation of I_{on} is related to both variations of $G_{m,max}$ and V_{th}. However, the I_{on} degradation is mainly caused by the deterioration of $G_{m,max}$ due to the similar degradation trends and magnitudes as shown in Figs. 2b and 3b.

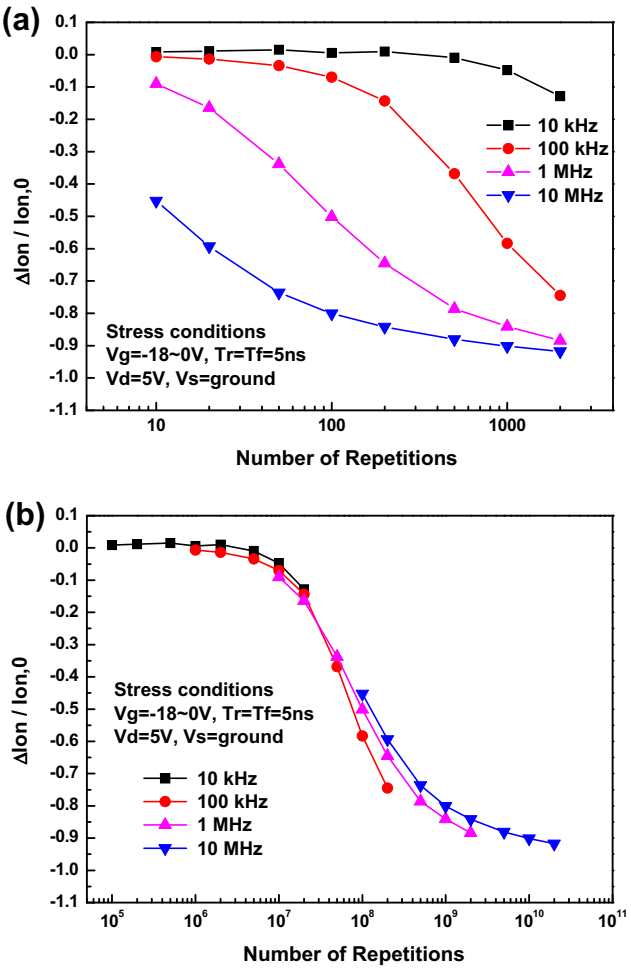

Fig. 2. Dependence of I_{on} degradation on the (a) stress time and (b) number of repetitions, under the stress conditions of V_g = −18–0 V, V_d = +5 V, source grounded, and $T_r = T_f$ = 5 ns at various frequency.

To investigate the dominant parameters of the applied pulse signals resulting in the degradation of $G_{m,max}$, we impose the pulse trains on the gate terminal with different combinations of T_r and T_f in the frequency 100 kHz and the stressing voltages are V_g = −18 to 0 V, V_d = +5 V, and V_s grounded. The transitional time dependence