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ScienceDirect

Energy Procedia 124 (2017) 331–337

Energy Procedia

www.elsevier.com/locate/procedia

7th International Conference on Silicon Photovoltaics, SiliconPV 2017

Towards an optimum silicon heterojunction solar cell configuration for high temperature and high light intensity environment

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Abstract

We report on the performance of Silicon Heterojunction (SHJ) solar cell under high operating temperature and varying irradiance conditions typical to desert environment. In order to define the best solar cell configuration that resist high operating temperature conditions, two different intrinsic passivation layers were tested, namely, an intrinsic amorphous silicon a-SiO_x:H with CO_2/SiH_4 ratio of 0.4 and a-SiOx:H with CO_2/SiH_4 ratio of 0.8, and the obtained performance were compared with those of a standard SHJ cell configuration having a-Si:H passivation layer. Our results showed how the short circuit current density J_{sc}, and fill factor *FF* temperature-dependency are impacted by the cell's configuration. While the short circuit current density J_{sc} for cells with a-SiO_x:H layers was found to improve as compared with that of standard a-Si:H layer, introducing the intrinsic amorphous silicon oxide (a-SiO_x:H) layer with CO_2/SiH_4 ratio of 0.8 has resulted in a reduction of the *FF* at room temperature due to hindering the carrier transport by the band structure. Besides, this *FF* was found to improve as the temperature increases from 15 to 45 °C, thus, a positive *FF* temperature coefficient.

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Peer review by the scientific conference committee of SiliconPV 2017 under responsibility of PSE AG.
10.1016/j.egypro.2017.09.307

Keywords: Silicon heterojucntion; temeprature coefficient; irradiance; current–voltage curve.

1. Introduction

Solar Photovoltaic (PV) price has been reduced by approximately 70% in the last five years. Recently, Dubai (United Arab Emirates UAE) has announced a record low bid of $58.5 per MWh for a 200 MW solar Photovoltaic (PV) project [1]. One of the key factors behind this low price is the direct dependency of solar PV performance on the operating temperature and irradiance conditions. The state of Qatar, for example, in the region of Middle East is highly rich of solar resource, on average a Global Horizontal Irradiance of 2113 kWh/m^2 was measured [2]. From the other side, a high operating temperature, on average a module temperature of 70 °C was measured during August, causes a drop in the PV module performance.

From our previous published work [3], the silicon heterojunction technology (SHJ) has shown a 10% increase in the energy yield at outdoor testing conditions as compared with conventional diffused-junction silicon technology. However, SHJ technology is known to suffer from parasitic absorption in the top layers [4]. In this paper, we address the approach of adapting the solar cell configuration, from one side to reduce the parasitic absorption, and from the other side to improve the solar cell performance at high operating temperature. We are proposing to replace the standard intrinsic amorphous silicon a-Si:H with a wider band gap amorphous silicon oxide a-SiO_x:H, which has the potential to reduce the absorption losses due to its superior optical transparency and therefore improving the short circuit current density J_{sc}. Our focus in this paper will be on the results obtained from the current-voltage (IV) measurements at different temperature and light intensity.

2. Experimental part

Three different SHJ solar cell configurations were studied, namely, the standard passivation intrinsic amorphous silicon (i) a-Si:H, and intrinsic silicon oxide layer (i) a-SiO_x:H with two carbon dioxide CO_2 to silane SiH_4 ratios of 0.4 and 0.8 (see Fig. 1). The fabrication steps of the SHJ cells were reported in reference [5]. The IV measurements were performed om a 2 x 2 cm^2 cells at different temperatures ranging from 15 to 65 °C in steps of 5 °C and for various irradiance conditions ranging from 0.05, 0.5, 0.75, 1, 1.5 and 2 suns, by using a homemade solar cell tester.

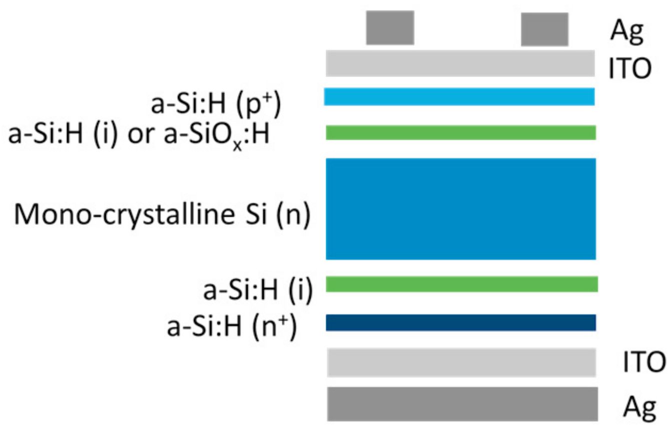

Fig. 1. Schematic of the silicon heterojunction solar cell under study. On the illumination side (top), Indium Tin Oxide (ITO) is used as an anti-reflective transparent conductive oxide layer. Current collection occurs through metallic (silver Ag) grid at the front and a stack of ITO and Ag at the rear. The schematic is not drawn to scale.

3. Results and discussion

In this section, first the open-circuit voltage (V_{oc}) and the fill factor (FF) as a function of temperature and