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ScienceDirect

Energy Procedia 124 (2017) 526–531

Energy Procedia

www.elsevier.com/locate/procedia

7th International Conference on Silicon Photovoltaics, SiliconPV 2017

Crack detection in crystalline silicon solar cells using dark-field imaging

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Abstract

The high capital expenditure (capex) necessary to manufacture crystalline silicon PV modules negatively affects the levelized cost of electricity (¢/kWh) and critically impacts the rate at which the PV industry can scale up. Wafer, cell, and module fabrication with thin free-standing silicon wafers is one key to reduce capex. Thin wafers reduce capex associated with silicon refining and wafer fabrication, which together sum to 58% of the total capex of silicon module manufacturing. In addition, thin wafers directly and significantly reduce variable costs. However, introducing 50 µm thin free-standing wafers into today's manufacturing lines result in cracking, creating a yield-based disincentive. Due to the brittle nature of silicon, wafer breakage is the major concern due to the high stress that is induced during processes in manufacturing lines. In this paper, we describe an improved method for edge micro-crack detection that can help enable low-capex, thin free-standing Si wafers. We present a method of detecting and measuring cracks along wafer edges by using a dark-field IR scattering imaging technique which enables detection of edge cracks at the micron scale.

Peer review by the scientific conference committee of SiliconPV 2017 under responsibility of PSE AG.

Keywords: Capex; polysilicon; thin free-standing wafer; edge crack detection; IR scattering; dark-field imaging

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1876-6102
Peer review by the scientific conference committee of SiliconPV 2017 under responsibility of PSE AG.
10.1016/j.egypro.2017.09.252

1. Introduction

One of the challenges in today's photovoltaic (PV) industry is the high capital expenditure (capex) to manufacture crystalline silicon PV modules, which comprises ~22% of the minimum sustainable price of PV modules [1]. In addition, nearly 52% of silicon capex is embedded in polysilicon and wafer manufacturing, negatively affecting the cost-per-watt ($/W), levelized cost of electricity (LCOE) (¢/kWh), and preventing the scale up of the PV industry (ref. [1] for the year 2015). To reduce this market limitation, approaches to reduce capex have been developed [2] and include: i) increase of tool throughput *e.g.* production volume and yield (m^2 per unit time), ii) improvement of solar cell conversion efficiency (W per m^2), and iii) reduction of silicon usage per wafer. Kerfless technologies represent a promising approach to reduce the required amount of silicon, since wafer with the same thickness can be produced with less silicon compared to the standard ingot-based growth methods.

In addition, since the silicon wafer is the largest cost component in finished solar cells, it is widely accepted that a reduction of silicon wafer thickness without a decrease in yield will lower solar energy costs [3,4]. By using thinner wafers in manufacturing lines, polysilicon and crystal growth capex is reduced (proportionally with grams-of-silicon-per-watt); therefore, thin silicon has the potential to reduce poly-to-module capex by roughly 45% (see Fig. 1). The total capex is shown as a function of Si wafer thickness, which was varied between 20 and 210 µm, assuming different manufacturing yields from polysilicon to the final module (92%, 80% and 65%).

Si wafer thickness has decreased steadily over the years, but not as quickly as predicted despite the agreed cost benefits of thinner wafers. Handling and processing thin Si wafers (40 - 100 µm) is difficult and manufacturing yield is unacceptably low. Since micro-crack defects are more critical in thinner wafers due to the lower breakage force [5], they can seriously impede the solar cell performance and reliability of the module. On one side, the reduced thickness of the wafer implies that the wafer is more flexible, which means that the deflection is higher for the same applied force [6]. On the other side, the mechanical stress which can be applied to the wafer before failure decreases with wafer thickness. As a result, a crack will propagate from a smaller in-plane tensile stress when a force is applied normal to the crack plane (known as mode I fracture) [7]. In order to decrease the breakage rate of thinner wafers, the requirements for reducing mechanical loads during processing steps (*e.g* sawing, interconnection of cells, handling and transport) have to be adjusted. In addition, inline edge crack detection tools have to be improved and/or new techniques must be developed to allow for a non-destructive, fast, and accurate method of crack detection and characterization for thinner wafers with a wide variety of crack types [8].

State-of-the-art technologies for crack detection in silicon materials include: photoluminescence (PL) [9], optical transmission [10,11], infrared (IR) lock-in thermography (LIT) [12], scanning acoustic microscopy (SAM) [13], and dark-field IR scattering [14]. Although all these techniques are suitable for detecting cracks within the wafer, they have several disadvantages for detecting edge cracks; especially cracks with less than a few millimetres in length. In particular, PL has difficulty detecting edge cracks since the technique is based on measuring the reduction in minority carrier lifetimes, yet at early stages in cell fabrication, the edges themselves reduce the local lifetime [9]. Optical transmission is challenging because it relies on reduced transmission when a crack is present; thus, the method inherently has a low signal-to-noise ratio (SNR) [10,11]. LIT is a powerful technique that utilizes IR photons to generate a specific temperature pattern, but only cracks with tiny tips and a triangular shape at the surface can be detected [12]. In SAM, the image is generated due to acoustic impedance mismatch caused by micro-cracks, but only cracks 5 – 10 µm can be detected, neglecting larger cracks [13].

Light scattering is a non-invasive technique which allows us to determine structures down to the sub-micron scale with a high SNR. Industrially-available tools detect edge micro-cracks down to ~3 mm in length. However, for thin wafers less than 150 µm, there is a need for detection of even smaller cracks in order to avoid breakage during cell and module fabrication. As shown by Ortner *et al.* [14], cracks smaller than 1 mm in length can lead to a breakage of 20% of the wafer somewhere in the module production line. Thus, there is still an industrial need for improving edge crack detection tools. Enabling these tools requires a better understanding of the underlying physics of crack detection in order to overcome these limitations.

Building on the industrially-available dark-field light scattering approach described in [14], the goal of this work is to establish a reliable method for detecting edge micro-cracks by exploring the trade-off between field of view (FOV), incident light angle, and detectable crack length. Our new approach shows the potential to be used as a