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Excellent via passivation and high open circuit voltage for large-area n-type MWT-PERT silicon solar cells

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Abstract

In this work, we improved the performance of the MWT-PERT solar cells focusing on increasing their V_{oc} by combining the MWT concept with *n*-PERT technology. The impact of different post-laser treatments on the via surface morphology and the via passivation was investigated. KOH texturing can partially remove the laser damage in the via and reduce the via SRV to 1000 cm/s. With optimized post-laser treatment and via passivation, an average V_{oc} of 685mV was achieved for our large-area *n*-type MWT-PERT cells. Front Ni/Cu plating and rear Ag and Al screen-printing were used for the metallisation, the compatibility of this hybrid metallisation scheme was studied. Using industrial solder-through interconnection technology, the cell was integrated in a laminate reaching a one-cell module efficiency at 20%. The reliability of the one-cell modules was preliminarily investigated in an extended reliability test.

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Keywords: MWT PERT solar cells; via passivation; plating; screen-printing; module reliability

1. Introduction

Crystalline silicon (c-Si) solar cells are currently dominating the photovoltaic market. Different approaches have been investigated to further improve the performance of crystalline silicon solar cells. One approach is to develop back-contact solar cells, such as Metal Wrap Through (MWT) structures [1], which requires only one additional

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processing step (laser via drilling) compared with standard industrial cell fabrication. With both contacts and interconnection at the cell backside, this design does not only reduce shading and absorption losses due to the reduced front metal coverage, which leads to a gain in the short-circuit current density (J_{sc}), but it also improves the aesthetics of the module. The advanced *n*-type PERT cell technology is another innovative approach featuring a dielectric passivation and local contacts on the rear side. Combining the features of the MWT and *n*-type PERT solar cells in an MWT-PERT solar cell architecture will result in a higher current due to minimized shadowing on the front, appealing aesthetics of the cells (no front busbars) and improved open circuit voltage (V_{oc}) due to a better rear passivation. An efficiency of 21% has been reported for large-area *n*-type homogeneous junction MWT PERT solar cells with V_{oc} of 656mV [2]. This champion cell features contacts with screen-printing of Ag and Ag/Al paste and unpassivated vias.

n-type PERT solar cells have demonstrated V_{oc} potential above 690mV in recent publications [3] [4]. In this work, we improved the performance of the MWT solar cells focusing on increasing their V_{oc} by combining the MWT concept with *n*-PERT technology. The impact of different post-laser treatments on the via surface morphology and the via passivation were investigated. KOH texturing can partially remove the laser damage in the via and reduce the via SRV to 1000 cm/s. With optimized post-laser treatment and via passivation, an average V_{oc} of 685mV was achieved for our large-area *n*-type MWT-PERT cells. A hybrid metallisation scheme was implemented in this work. Front Ni/Cu plating and rear Ag and Al screen-printing were used for the metallisation of our MWT-PERT solar cells to reduce the precious Ag consumption and cost. Two main challenges were previously identified for this hybrid metallisation scheme [5]. First, it is difficult to plate continuous fingers near the via printed-through Ag paste, which can prohibit a good contact. Second, for immersion plating tools, the adhesion of the Ag pads after exposure to plating solutions can be severely degraded. Thus, the integration of the hybrid metallisation scheme was investigated in this work, especially on the compatibility of the screen-printing pastes with the plating sequence. Finally, we integrated a number of cells into one-cell laminates using the solder-through interconnection technology [6] and subjected them to an extended reliability test.

2. Approach and experiment plan

2.1. Short-loop test and process optimization

Via passivation and metallisation integration were investigated using short-loop tests. To investigate the via passivation, symmetrical lifetime samples with different via densities were fabricated. After via drilling, a post-laser treatment was applied to remove the laser damage, using KOH saw damage removal (SDR) or KOH texturing. All the samples received then a front surface field diffusion (FSF) and were passivated by a dielectric stack of thermal SiO_2 and PECVD SiN_x on both sides. The process flow and structure of the samples are shown in Fig. 1. (a) and (b). The surface morphology of the via was studied by top-view and cross-sectional SEM, and the lifetime of the samples was measured using BT imaging. The samples were further received a laser doping on the front and screen-printed with Ag via paste on the rear. And the front contact was plated. The via paste printing and firing were well optimized to ensure the solderability of the rear Ag pads after the Cu plating. The adhesion of the Ag pads after soldering was measured by a 45° pull test.