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Impact of annealing on the formation and mitigation of carrier-induced defects in multi-crystalline silicon

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Abstract

Carrier-induced degradation (CID) of multi-crystalline silicon (mc-Si) wafers is a major problem currently affecting the photovoltaic industry. A large number of studies investigating this phenomenon have provided important clues regarding the identification of the defect, however, as of yet, none have isolated a specific cause. In this work, we provide further insight into the kinetics of CID in mc-Si by presenting a detailed study of the impact of dark annealing on the formation and subsequent mitigation of the carrier-induced defect. Previous work has shown that such anneals can modulate the kinetics of the defect. Here, we extend that work and demonstrate that dark annealing can result in accelerated defect formation and extended degradation throughout a subsequent light soaking cycle, irrespective to when the dark annealing was applied. It is suggested that dark annealing could release extra defect precursors into mc-Si, which then become recombination active upon illumination. Therefore, the subsequent degradation after dark annealing might not necessary involve a reverse reaction. Through multiple dark anneal and light soak cycles, the extent of degradation in each cycle continues to reduce. A direct reverse reaction (de-stabilisation) alone does not explain this observation. We suggest that this effect could be explained by the presence of a reservoir of defect precursors, which are gradually depleted throughout the dark annealing processes. Finally, it is demonstrated that dark annealing alone could potentially cause a similar degradation to illumination at elevated temperature.

Keywords: LID; CID; multi-crystalline silicon; dark anneal; defect precursors

1. Introduction

Multi-crystalline silicon (mc-Si) solar cells suffer from substantial degradation effects when subject to light or current injection, and this has been the focus of numerous recent studies [1]–[5]. This degradation is a serious issue for the photovoltaic (PV) industry since mc-Si PERC cells are predicted to become the dominant technology in the

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next decade [6]. The extensive time required for the material to degrade and eventually recover under field conditions [4] and the severity of the degradation (up to 16% relative power loss [7]) leads to a significant loss in total energy yield. Since the degradation can be triggered by carrier injection either from illumination or bias voltage [8], the degradation will be referred to in this paper as mc-CID, rather than light and elevated temperature induced degradation (LeTID), as it is commonly called [2].

Despite significant research efforts, the root cause of mc-CID has not yet been identified. One of the difficulties in understanding mc-CID is the lack of a kinetic model that can explain experimental results. In contrast, a three-state model has been developed for boron-oxygen carrier-induced degradation (BO-CID) [9]. The development of that model has greatly facilitated understanding of the defect behaviour, been useful in the modelling of experimental results, and has enabled predictions of future performance [10]–[12]. However, the applicability of the three-state model in describing the kinetics of mc-CID to date, has been less thoroughly studied. In mc-CID, illumination at elevated temperature causes a degradation and subsequent recovery of minority carrier lifetime, which matches the forward reaction of defect formation and subsequent defect passivation in the BO-CID model. There have been numerous studies into this forward reaction for mc-CID, such as the mechanism of defect formation [13]–[17] and accelerated passivation [8], [18]. However, the reverse reaction has rarely been mentioned in the literature. Annealing at the degraded state has been described as dissociation in analogy to the three-state model [18]. In another study, a degraded wafer underwent dark annealing during the formation of passivation stacks. The wafer was recovered but degraded again upon exposure to light. Hence, it was concluded that mc-CID is reversible by annealing [15]. In contrast, it has also been shown that annealing at the degraded state could only partially recover the open circuit voltage of mc-PERC cells [16]. In addition, the degradation rate during the second degradation cycle was faster than that of the initial degradation cycle. Thus, it was suggested that the state after annealing is different from the initial state before any defect formation. Recently, we have demonstrated that a pre-dark anneal process could significantly alter the kinetics of the defect formation in mc-PERC cells [19]. However, in this case, the potential impact of changes in surface recombination could not be separated from defect formation within the bulk. Similarly, it was recently proposed that SiN_X passivation may be unstable under the conditions and long process times used to form the mc-CID defect [20].

This paper studies the kinetics of formation and mitigation of the defects responsible for mc-CID. It presents a detailed investigation of the impact of dark annealing (applied at various stages) on subsequent degradation. It is observed that dark annealing resulted in extended degradation and accelerated defect formation irrespective of the as-fired defect state. Furthermore, it is demonstrated that the maximum extent of degradation can be reduced when the sample was cycled between the dark annealed and light soaked states. The work also investigates the possibility that surface passivation from SiN_X could be unstable during dark annealing or illumination via Shockley-Read-Hall statistical analysis performed at various stages to separate the impact of bulk and surface recombination on the total effective lifetime.

2. Experimental

The impact of dark annealing on the kinetics of mc-Si defect formation and mitigation was studied by creating symmetrical lifetime structures on sets of 'sister' samples. The carrier lifetime of the samples was monitored periodically during accelerated defect formation cycles with thermal hotplate annealing being applied at different stages. Test samples were fabricated on 1.3 Ωcm p-type mc-Si, selected from neighbouring locations to provide sets of 'sister' samples. The wafers underwent acidic texturing to a final thickness of about 180 μm. The samples were diffused in a $POCl_3$ tube furnace to result in a 70 Ω/□ emitter on both sides. SiN_X with a thickness of 75 nm and a refractive index of 2.08 at 633nm was deposited on both sides using PECVD [21]. Finally, the wafers were fired in a belt furnace with a 740 °C peak wafer temperature, which has been shown to trigger mc-CID [22]. All sister samples are assumed to behave in a similar way, given that the crystallographically identical wafers received identical processing.

The light soaking (LS) process was carried out using a previously validated accelerated technique [8]. The illumination was provided by a 938nm laser, which resulted in an irradiance of approximately 2.6 W/cm^2. Temperature control during the LS process was achieved by processing the sample on a hotplate with vacuum suction. The hotplate temperature was measured as 122 °C during LS and was monitored by an infra-red temperature