Microelectronic Engineering 88 (2011) 877–881

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Ultradense silicon nanowire arrays produced via top-down planar technology

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ARTICLE INFO

Article history:
Received 13 August 2010
Accepted 19 November 2010
Available online 13 December 2010

Keywords:
Silicon nanowires
Top-down processing
Electrical characteristics

ABSTRACT

A process is developed for the fabrication of vertically arranged poly-silicon nanowires via a rigorously top-down batch process. The technique allows the production of wire arrays with larger linear density (projected on the surface) than those achievable with any of the other proposed top-down processes.

1. Introduction

Semiconductor nanowires (NWs) have attracted a large interest in the past years [1–4] for their potential applications in electronics [5], optoelectronics [5], and medicine [6–8].

Silicon NWs, in particular, have been the focus of an increasing interest [9,10] because of their integrability in silicon-device processing. Far from being complete, the list of potential applications includes biochips [11], new-generation electronics [12,13], conductive wires defining the crossbars for molecular electronics [14,15], demultiplexing elements for sublithographic crossbars [16–18], and active elements of Seebeck generators [19,20].

Some of the above applications require single crystalline silicon; for others (those exploiting the majority carriers) poly-crystalline silicon is sufficient (as happens for conductive wires for hybrid inorganic–organic crossbars [14–16]) or even better (as in the case of almost degenerate nanowires as Seebeck generators [19,20]). In this work, the attention will be concentrated on poly-crystalline silicon (poly-Si), of which we exploit its ability to give conformal coverages even in very restricted geometries when deposited from silane monomers at low pressure.

Of course, NWs may be prepared using lithographic methods: conventional photolithography (henceforth 'lithography' without attributes) combined with controlled overetching allows their cheap production, but the maximum linear density is limited to 10^5 cm^{-1} by the achievable pitch P of about 100 nm; advanced (electron beam, deep ultraviolet, or extreme ultraviolet) lithography allows the density limit to be extended by a factor of 5–10, but at a huge production cost (due to investments for deep or extreme ultraviolet lithography, or to low throughput for electron-beam lithography).

If the intended application of poly-Si NWs is consistent with their arrangement in regular arrays, the simple geometry allows them to be prepared via much cheaper non-lithographic techniques (NLTs). These NLTs are generally based on the *transformation of a thickness into a width*. This operation is convenient when

(i) the thickness is controllable on a length scale much smaller than the lithographically producible length scale W, and
(ii) the process keeps the width w close to the thickness t of the film.

Situation (i) is characteristic of many films, whose thickness is controllable on the nanometre length scale whereas the lithographic definition is on the length scale of 10^2 nm. Since now on we shall limit to situations satisfying both (i) and (ii), for which non-lithographic features are sublithographic features:

$$\mathrm{NLT}: t \overset{w \simeq t \ll W}{\rightarrow} w,$$

where the sizes of sublithographic features are denoted with lowercase letters, whereas those of lithographically defined features are denoted with the same capital letters. We shall conform to this convention even in the following.

Among the NLTs we mention the *superlattice nanowire pattern transfer* (SNAP) technique that may be used for the preparation of masks for a subsequent nanoimprint lithography (NIL), and the *multi-sidewall patterning technology* (MSPT) that instead requires a preliminary pattern defined lithographically.

Nanoimprint lithography is a technique for the one-to-one transfer of a pattern from a contact mask to a substrate without using optical projection [21,22]. This technique is emerging as a

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doi:10.1016/j.mee.2010.11.034

potential successor of advanced lithography because of its simplicity, low cost, high throughput, and high resolution [23]. The reduced complexity of NIL apparati is paid in terms of the difficulty of preparing hard masks with adequate quality. If NIL is addressed to define NWs (rather than to impart a specific shape to the imprinted pattern), the mask can conveniently be produced via SNAP technique. The SNAP is an NLT for the preparation of NIL masks for nanowires [24]. For instance, a contact mask with pitch p of 16 nm was prepared growing a superlattice on a single crystalline substrate by molecular beam epitaxy, cutting the sample perpendicularly to the surface, polishing the newly exposed surface, and etching selectively the different strata of the superlattice [25].

The MSPT, instead, is essentially based on the repetition (in additive or multiplicative fashion) of the sidewall patterning technique (SPT), an age-old technology originally developed for the dielectric insulation of source-and-drain metal electrodes from the gate of field-effect transistors [26–33]. Wire arrays with pitch p on the length scale of 20 nm seem at the reach of this technology: nanowires with width of 7 nm [27] and arrays with $p = 35$ nm have indeed been reported [28,29].

If p is the pitch of the NW array (as results from SNAP-NIL or MSPT), the linear density δ is given by $\delta = p^{-1}$. Higher densities are producible, for assigned pitch, only arranging the NWs not only horizontally but also vertically. As far as the NW arrays resulting from SNAP-NIL and MSPT lie in a plane, these techniques succeed in the production of higher densities only arranging the NW arrays in more layers. The production of N layers requires however the repetition of N unit operations and, consequently, the multiplication of production cost by the same factor (and likely implies a loss of yield).

In this work, we shall demonstrate that a vertical organization of the NW arrays is possible via a non-conventional use of otherwise fully conventional planar technology. The demonstration will be carried out preparing three-dimensional arrangements of poly-Si nanowires, where the NWs are disposed with vertical separation on the 30-nm length scale and horizontal separation on the deep sub-micrometre length scale.

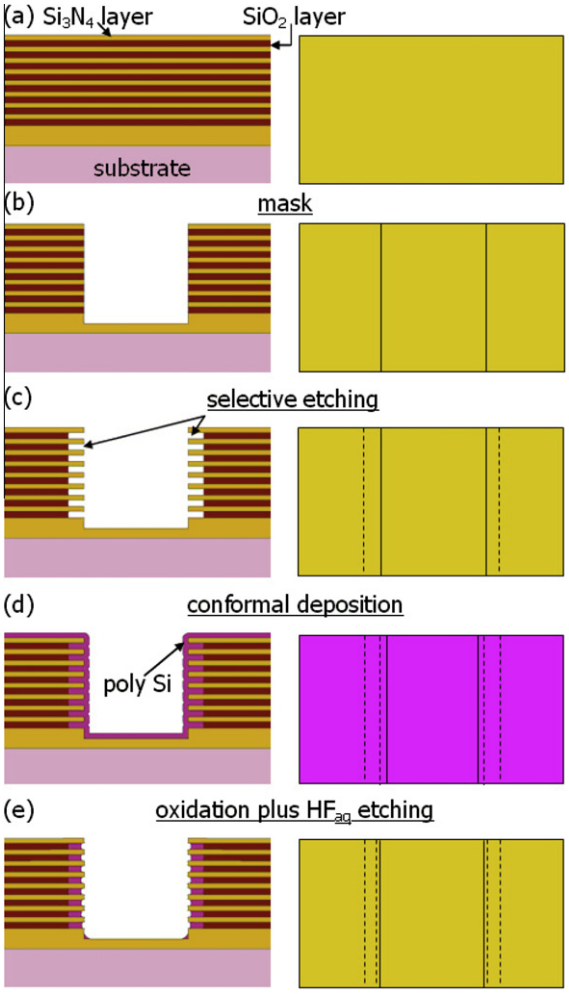

Fig. 1. Cross-sections (left) and plan views (right) of the structures resulting in the preparation of the vertical wire arrays.

2. Vertical organization of the nanowire array

The basic idea consists in the exploitation, by controlled etching and filling, of the recessed regions resulting from conventional IC processing [34].

2.1. Sketch of the idea

The process starts with the formation of a multilayered stack of insulators A and B over a suitable insulating substrate C as sketched in the following:

$$\mathrm{C}\|\underbrace{\overbrace{\mathrm{A}|\mathrm{B}|}^{1}\overbrace{\mathrm{A}|\mathrm{B}|}^{2}\cdots\overbrace{\mathrm{A}|\mathrm{B}|}^{N}}_{t_N=N(t^{\mathrm{A}}+t^{\mathrm{B}})}, \tag{1}$$

where t^{A} and t^{B} are the thicknesses of films A and B, while t_N is the thickness of the stack: $t_N = N(t^{\mathrm{A}} + t^{\mathrm{B}})$. The materials are characterized by the existence of a selective etch for A with respect to B; C may coincide with A or B. To be concrete we shall think of A as SiO_2, of B as Si_3N_4, and of C as a thick SiO_2 layer.

The thicknesses of A and B are not critical; however for reasons of concreteness we shall fix them to $t^{\mathrm{A}} = 30$ nm and $t^{\mathrm{B}} = 20$ nm, respectively. The number N of bilayers forming the film is such to allow the formation by directional etching (e.g., via reactive ion etching, RIE) of a deep trench with depth t_N.

The overall process, sketched in Fig. 1(a)–(e), involves the following steps:

(a) sequential deposition of N SiO_2—Si_3N_4 bilayers,
(b) definition thereon of a deep trench,
(c) formation of N recessed regions per trench side by partial selective etching of the SiO_2 layers,
(d) conformal deposition of a poly-Si film sufficiently thick to fill completely the recessed regions, and
(e) partial selective etching of the poly-Si film for the duration required to etch silicon from the horizontal regions.

2.2. Proof of the idea

The process was practically implemented starting from n-type silicon (100) wafers with resistivity of 0.2—1 Ω cm and initiated with the growth via wet oxidation at 1000 °C of an SiO_2 layer with thickness of 120 nm.

After that an Si_3N_4 film with thickness of 50 nm was grown by low-pressure chemical vapour deposition (LPCVD) at 780 °C in SiH_2Cl_2 and NH_3 atmosphere and partially oxidized at 1100 °C in wet atmosphere in order to create a thin SiO_2 layer. The reiteration of this procedure produced a stack of alternating Si_3N_4 and SiO_2 layers.

This stack was patterned using conventional photolithography and a reactive ion etching RIE.

A diluted water solution of HF ($HF : H_2O = 1 : 20$ vol./vol.) was used for the selective etching of SiO_2 and the duration of the etch