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An Optimal design of 2-to-4 Decoder circuit in coplanar Quantum-dot cellular automata

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Abstract

Quantum-dot Cellular Automata (QCA), an emergent nanotechnology which promises to deals with the limitations of CMOS technology. This technology offers very low power operation of digital systems with high speed. This paper represents an efficient 2-to-4 decoder, which has been designed with the help of three-input majority voters and successfully implemented in QCA. The design is optimized by considerably reducing the number of cell counts and QCA wire crossings. The proposed decoder is more robust and enjoys single layer wire crossing, via clock phasing, which requires only one type of cell .The results shows that the proposed decoder circuit performs equally well compared to existing decoder designs and performs better in case of previous coplanar decoder designs with enable input functionality in all aspects. Our design achieves 41% and 28% improvement in number of cell counts and 43% and 42% area improvements in comparison to the existing five input and three input based majority gates decoder designs respectively, which have presented in this paper. QCA Designer tool is used to validate the layout of the proposed designs.

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Key Points: Quantum-dot cellular automata(QCA); Majority gate; QCA Designer; Decoder

1. Introduction

A motivation towards nanotechnology is due to the limitations of scaling down of MOS structure in CMOS technology, because the scaling down of MOS leads to an increase in operating powers and latency. Also, at the same time there are numbers of problems like short channel effects, tunnelling effects etc. have been discovered, which have encouraged the need to find an alternative of CMOS technology. Quantum-dot cellular automata (QCA) is one of the alternative nanotechnologies that is proposed to overcome such problems and take over the CMOS circuit designs. This technology offers low power operation and high speed of digital circuits in comparison to current CMOS technologies based circuit designs. Decoders are important digital circuit, which is generally used for addressing random access memory arrays. They can also be design in Quantum-dot cellular automata (QCA) technology at Nano scale. Previously, a number of decoder designs have been proposed, but no one are actually efficient.

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A number of QCA decoders have been designed and implemented with the help of different majority gates. For Example in Fig. 4. they have implemented a decoder with enable input based on 3 input majority gates, during the design of Look up Table, a part of combinational logic block (CLB) of field programmable logic array (FPGA). Also in Fig. 5. they implemented a 2-to-4 decoder, which is based on five input majority gate with the aim of reducing the complexity of design structure. This approach results in large unused area which can be seen from comparison table [2].

The organisation of this paper is as follows, in section 2, QCA preliminary have discussed. In section 3, Proposed QCA decoder is presented. Section 4 represents QCA implementation of proposed decoder and its simulated output .Section 5, represents comparative study analysis of proposed decoders with existing one in all aspects. The last section 6, represents the conclusion.

2. QCA Preliminary

2.1. QCA Basics

All QCA devices is basically designed with the help of "QCA cell", which is shown in Fig. 1(a). As from the figure we can see that, QCA cell is basically square in shape which comprises four quantum dots and two free electrons. Each quantum dots are separated from others by barriers called tunnelling barriers. These tunnelling barriers are raised and lowered by application of clock so that electrons can hold its antipodal sites and tunnel between dots respectively. Since these electrons faces columbic force of repulsion from each other, so they always try to occupy the largest possible distant sites i.e. opposite corners, which represents two type of polarizations.

The basic example of QCA logic devices implementation are QCA wire, inverter, and majority voters as presented in Fig. 1.QCA wire is generally implemented by cascading of QCA cells shown in Fig. 1(b), through which binary data will be propagate, through columbic interactions. Another basic device for digital logic i.e. inverter is built by just placing the QCA cells in a diagonal manner as shown in Fig. 1(c); or in general, it can also be implement by help of seven cells placed appropriately as shown in Fig. 1(d). The output *'out'* of the inverter gets polarized in opposite manner of the polarization of QCA cell input *'in'*. Now QCA majority voter (MV) and its logical representation are shown in Fig.1(e), which represents three input majority voter whose logical function is described as F(A,B,C)=AB+AC+BC. It is termed as majority because the output will be decide on the basis of polarization of majority of inputs. This majority voter is implemented with the help of just five cells placed like cross structure. The input Cells are termed as Cells A, B, and C whereas the Cell D acts as the output cell whose polarization depends upon the polarization of majority of input cells as discussed earlier. For example, if two (out of three) QCA cells inputs are polarized to -1. The output cell of majority voters will also gets polarized to -1, as shown in Fig. 1(e). These majority voters can also function as Logical OR and AND operation by inserting one of its inputs cells to binary values 1 and 0, respectively.

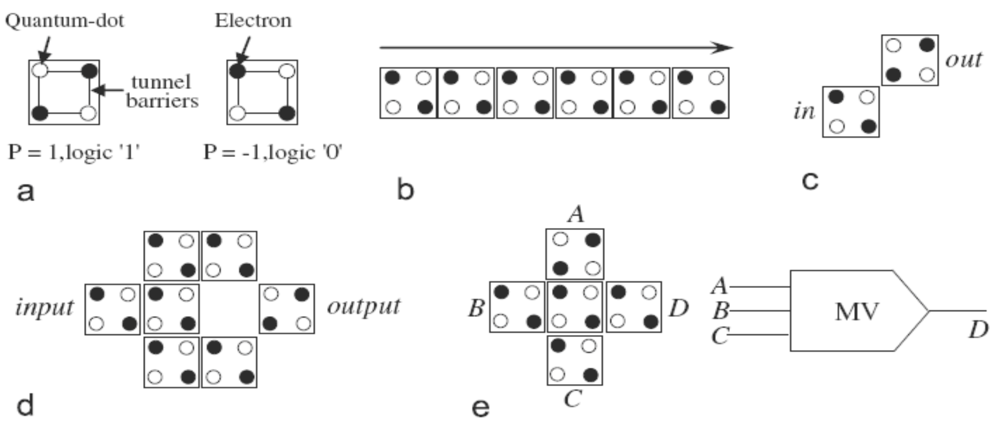

Fig. 1. Basic digital logic devices in QCA(a)QCA cell; (b) QCA wire; (c)and(d) QCA inverter; (e)Majority gate or voter(MV)