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Numerical simulation of the electrical performance of printed circuit boards under cyclic thermal loads

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ABSTRACT

Different Printed Circuit Board (PCB) designs were tested in an Interconnection Stress Test. In such a test, PCBs were subjected to temperature cycles alternating between two extremes (e.g. −40 °C to 160 °C). The electrical resistance was measured on-line during these tests. If the resistance rose by more than 10% of the initial value at the highest temperature, the test was terminated. The PCB structures were modeled by means of the Finite Element Analysis (FEA) Software Abaqus using a viscoplastic material model extended by a mean backstress memorization for the domain representing the copper interconnections. The stress/strain states computed by Abaqus served as input to a pore growth model which eventually allowed working out an indicator for the electrical performance loss. Subsequently, electrical FEA were conducted to obtain a correlation between the pore volume fraction distributed over the structure and the electrical resistance increase. The results of the simulations were compared to experimental results to determine parameters for the pore growth model. A well calibrated pore fraction evolution law allowed reliably predicting the electrical performance of various PCB designs as well as drawing some conclusions on the initial pore volume fraction in the PCB prior to operation.

1. Introduction

Printed Circuit Boards (PCBs) are composite structures made of electrically conducting materials like copper and electrically insulating materials like FR4-prepregs and -cores. These terms refer to glass fiber-reinforced epoxy resins. As these materials show different coefficients of thermal expansion, stresses arise when PCBs are thermally loaded. Cyclic thermal loading is a frequent loading case which can occur in consumer electronics, e.g. mobile phones which are used at different temperatures, as well as for technical systems such as motor control systems. Since cyclic thermal loading can lead to a degradation of the electrical properties and subsequently to circuit failure, there are industry-wide standards to test the reliability of PCBs under these conditions [1,2,3,4]. To save costs for prototypes and testing, researchers and scientists are constantly improving simulation and modeling techniques for electronics [5,6,7,8]. As cyclic thermal loading is a fatigue issue, material models reproducing the constitutive behavior under cyclic loading as well as a description for damage evolution are needed. Existing literature either provides input data for the constitutive and damage modeling of the prepregs and cores [9,10] or focuses on the modeling of the solder [11,12]. Additionally, literature dealing with thermal management for PCB design is available [13,14]. Besides, literature distinguishes between homogenized [15] and localized approaches, the latter being the appropriate choice for damage consideration. This research work offers a damage model for the copper vias. Furthermore the question is tackled to what extent mechanical damage correlates with degradation of the electrical performance. To the authors' best knowledge, there is currently no literature dealing with mechanical-electrical simulation of PCBs available. In a previous work a methodology to test thin copper layers under cyclic tension-compression loads at different temperatures [16] was developed. Due to the small dimensions of copper layers used in PCBs, they could not be tested stand-alone, but had to be bonded to substrates. Subsequently, the parameters for the isotropic and kinematic hardening behavior were determined [17] and fed into a suitable constitutive material model [18]. In addition to this work, monotonous temperature-dependent tensile tests on FR4-prepregs were conducted [19,20,21].

This work focuses on the copper vias that form the current paths. Their reliability is crucial to the functionality of whole devices. Hence the presented research provides a numerical methodology to test new circuit designs of PCBs under cyclic thermal loading conditions. Interconnection Stress Tests (IST) [22,23] of different PCB designs were conducted to provide the experimental basis of this work. In such tests, PCBs were subjected to temperature cycles alternating between two extreme (e.g. −40 °C to 160 °C) temperatures. The electrical resistance was measured online during these tests. If the resistance rose to more than 10% of the initial value at the highest temperature, the test was

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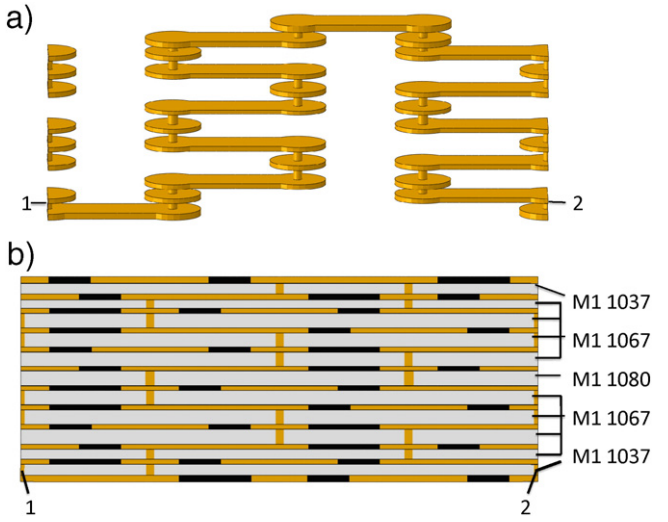

Fig. 1. Microvia-test design: (a) investigated copper path, (b) layer built-up.

terminated. Simultaneously, finite element models of these designs were set up in the commercial software Abaqus (Simulia, Daussault Systèmes, Providence, RI, USA). For the material description the constitutive model for thin copper layers developed in a previous work [18] was implemented and a pore growth indicator was added. Pore growth was chosen as a damage indicator, because the relationship between pore volume and electrical resistance is known from the literature [24]. It was thus used to establish a link between the mechanical and the electrical simulations (see Chapter 3). In order to save a considerable amount of computation time and to be able to determine the parameters of the pore growth model, the damage simulations were done based on a stabilized loading cycle. To this end, the stress-strain state at a stabilized cycle was exported from Abaqus and pore growth was calculated by means of an external Matlab-Script (Natick, MA, USA). Separating the mechanical analysis from the pore growth calculations is admissible as long as the pore volume fraction does not feed back to the elastic data which has been assumed here for the sake of simplicity. The so-calculated local pore volume fraction was then re-imported into Abaqus by means of a user subroutine (User Defined Field UFIELD) [25] for the subsequent electrical simulations obviously significantly affecting the conductance properties of the current paths. That way, a virtual IST could be performed using a decoupled mechanical-electrical FEA.

2. Material models

2.1. Constitutive modeling

2.1.1. Modeling of the copper parts

For modeling the constitutive behavior of thin copper layers the "nonlinear isotropic/kinematic hardening model" implemented in Abaqus [26] was employed. It is based on the work of Lemaitre and Chaboche [27,28]. It can reproduce the behavior of ductile metals subjected to cyclic loading. The elastic region is assumed to behave linear-elastically following Hooke's law, the plastic behavior is described with classical Mises concepts. In the tests a correlation between the yield stress of the stabilized cycle Q and the mean force was observed. In the material model this effect was accounted for by introducing a further internal variable c memorizing the mean stress [17,18]. As the backstress tensor $\boldsymbol{\alpha}$ marks the center of the elastic region, the first invariant of the backstress $I_1(\boldsymbol{\alpha})$ was integrated over a certain timespan. The time elapsed until a certain amount of equivalent plastic strain is reached ($\bar{\varepsilon}^{pl}$) was used. Finally, the so-obtained value was divided by the duration of one loading cycle T. Eqs. (1) and (2) show the formalism, Q is the yield stress of the stabilized cycle, D and g are material

$$c = \frac{1}{T}\int_{t\left(\bar{\varepsilon}^{pl}=0\right)}^{t\left(\bar{\varepsilon}^{pl}=\bar{\varepsilon}^{pl\_limit}\right)} (\boldsymbol{\alpha})dt \quad \text{with} \quad I_1(\boldsymbol{\alpha}) = \alpha_{11} + \alpha_{22} + \alpha_{33} \tag{1}$$

$$Q = D(T)e^{-g(T)|c|} \tag{2}$$

parameters. For practical reasons the Q versus c curves were truncated with the highest value for Q recorded at a given temperature. The temperature-dependent coefficient of thermal expansion (CTE) for the used copper grade was determined in [19].

2.1.2. Modeling of the dielectrical parts

In PCBs both glass fiber-reinforced epoxy resins (cores and prepregs) as well as the pure resin are utilized. The cores and prepregs were modeled using temperature-dependent orthotropic elasticity, for the pure resin a temperature-dependent isotropic elastic model was used. The elastic properties were measured temperature-dependent by Dynamic Mechanical Analysis (DMA). Additionally, all of them were characterized in tensile tests at room temperature. From these measurements the Poisson's ratios were taken as they cannot be measured in the DMA and tensile tests at different temperatures are very time-consuming. For the cores and prepregs the out-of-plane mechanical properties had to be calculated by micromechanics simulations. The

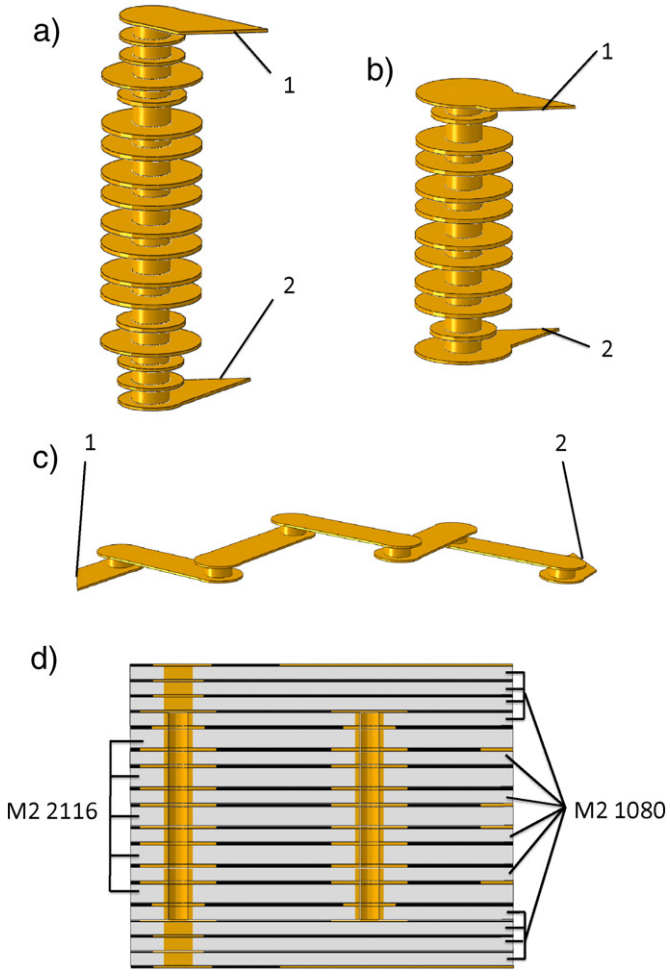

Fig. 2. a) Through hole b) buried via and (c) line structure test-design d) layer build-up.