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Wireless inter-chip interconnects

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ABSTRACT

Inter-chip wireless interconnect technologies such as inductive coupling and electromagnetic wave propagation have been developed for future high performance system in package at low cost. Inductive coupling is used for near field transmission whose distance is shorter than 100 μm as local wireless interconnects. Antennas are used for far field transmission between chips whose distance is longer than 1 cm as global wireless interconnects. A single-chip Gaussian monocycle pulse (GMP) transmitter using complementary metal oxide semiconductor (CMOS) technology with an on-chip integrated antenna was developed for inter-chip ultra wideband (UWB) communication.

1. Introduction

According to the scaling rule for metal-oxide-semiconductor (MOS) transistors in silicon large scale integrated circuits (LSI), both operating frequency and power consumption can be improved by reducing the feature sizes of MOS transistors [1]. Therefore, system on a chip (SOC) has been developed because of its highest transistor density. However, disadvantages of SOC are high non-recurring engineering (NRE) cost, high cost for low volume and long time to market. Furthermore, the scaling of metal interconnects in SOC deteriorates the performance of the LSI in terms of operating frequency and power consumption because it increases resistance–capacitance (RC) time constants [2]. To reduce the RC delay, the copper (Cu) interconnect and low-dielectric constant (low-k) materials have been developed for 90 nm CMOS and beyond [3]. Although the Cu/low-k technology can solve the existing problems, it cannot be an ultimate solution for total systems as far as they are used for SOC.

Nowadays, time to market and integration at low cost are the most important concerns in semiconductor industries. From this point of view, system in a package (SIP) has been developed because of its short time to market and low NRE cost. However, disadvantages of SIP are lower integration density compare to SOC and long interconnect lengths of wire bonding and global interconnects on a printed circuit board (PCB). Conventional integration systems of LSI on a board using bonding wires limit the high-speed and high bandwidth transmissions between LSI chips due to their parasitic inductances (L) and capacitances (C).

Therefore, three dimensional (3D) stacked chip integration has been developed to solve these problems with low cost and low power dissipation. To substitute wire bonding, through-silicon via (TSV) [4,5] and micro bump technologies [6] have been developed for 3D integration to minimize the interconnect length and continue Moore's law. However, cost and yield problems due to its process complexity and screening of known good die (KGD) for TSV must be solved for mass production.

Wireless inter-chip interconnects such as capacitive coupling [7–9], inductive coupling [10–20] have potential to solve the wire bonding problems in terms of cost and yield as well as high frequency performance. Since transmission ranges of capacitive and inductive couplings are less than a few μm [9] and a few tens μm [16], respectively, they are suitable for clock and data communications between adjacent chips. On the other hand, the electromagnetic wave transmission using on-chip antennas can reach further distance than 1 cm so that it can be applied to inter-chip re-configurable interconnections. A three-dimension custom stacked system is proposed for both local wireless interconnects (LWI) between adjacent chips using inductive coupling and global wireless interconnects (GWI) among separate chips using electromagnetic wave propagation as shown in Fig. 1 [12]. The target distances of LWI and GWI are a few hundred μm and a few cm, respectively.

Among wireless interconnection technologies, inductance coupling and transverse electromagnetic (TEM) wave propagation are investigated. Fig. 2 shows transmission coefficients of inductive

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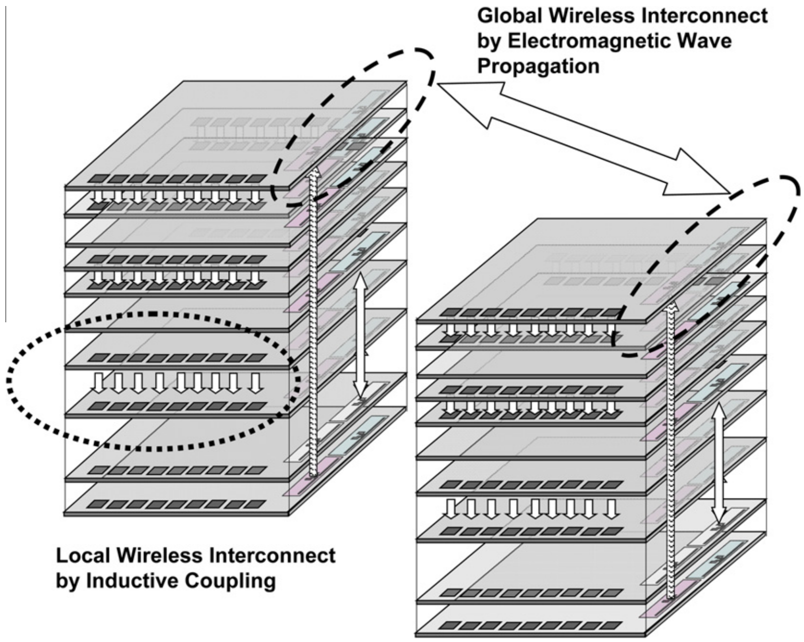

Fig. 1. Schematic diagram of inter-chip wireless interconnection for three dimensional stacked LSI chips. Global wireless interconnects by use of electromagnetic wave propagation and local wireless interconnects by use of inductive coupling are implemented.

coupling by use of loop inductors and TEM wave propagation by use of half-wavelength dipole antennas as a function of distance.

The transmission gain (S_{21}) of the loop inductors, whose total length is 4.94 mm, decreases in inversely proportion to the square of distance (R) which is normalized by a wave length (λ). The S_{21} deceases abruptly with distance not only in the far field ($R/\lambda > 1/2\pi$) but also in the near field ($R/\lambda < 1/2\pi$).

Fig. 3 shows a photograph of 3D integration chip for object detection and recognition with global and local wireless interconnects [13].

2. Inductive coupling

Fig. 4(a) illustrates inductive coupling between spiral inductors on stacked silicon chips. Conductivity of a Si substrate is an obstacle for inductive coupling between two spiral inductors so that the

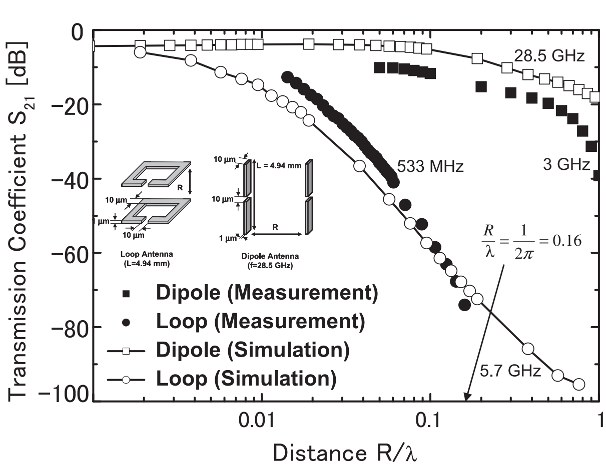

Fig. 2. Transmission coefficients (S_{21}) versus normalized distance for inductive coupling by use of loop inductor and electromagnetic wave propagation by use of half-wave dipole antenna. $R/\lambda = 1/2\pi$ is the interface between near field and far field.

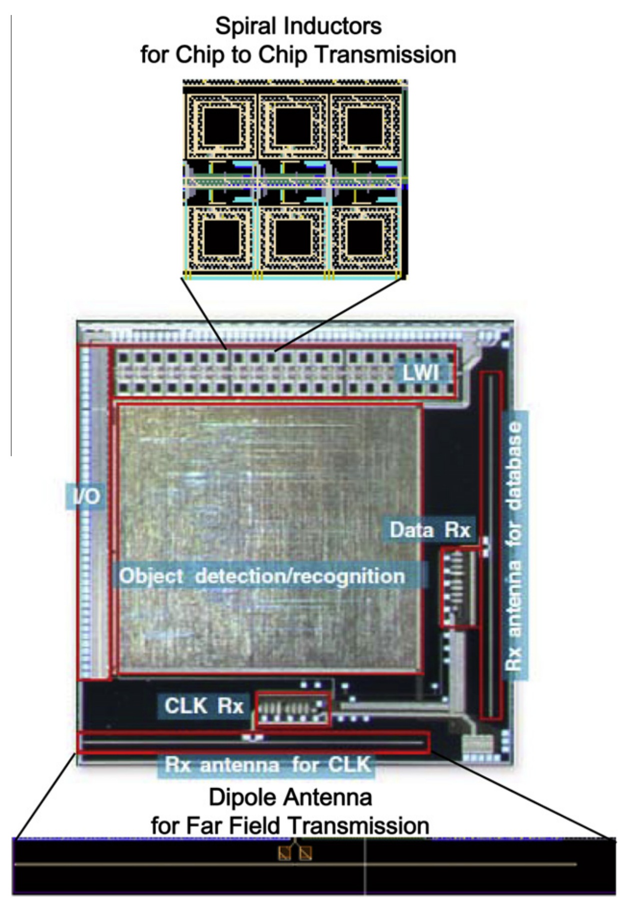

Fig. 3. Chip photomicrograph of 3D integration for object detection and recognition with global and local wireless interconnects. Spiral inductors are used for chip to chip transmission. Dipole antennas are used for far field transmission.