

FinFET-based product performance: Modeling and evaluation of standard cells in FinFET technologies



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ABSTRACT

Technology scaling has an increasing impact on the resilience of integrated circuits. This leads to the necessity of using new technology-level innovations, such as employing FinFET instead of planar transistors. For such novel devices, performance characteristics, reliability and variability behave potentially different, compared to planar devices. This paper explores different sources of process variations in 14 nm technology node and studies their impact on FinFET-based circuit designs. Both TCAD and PTM device models are used and compared with regard to the performance metrics of the circuits. This reveals insights into the behavior of future technology generations. Reliability and variability will be considered.

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1. Introduction

With continuous downscaling of technology nodes, reliability has become an increasingly important concern for CMOS devices. Shrinking of feature sizes to achieve less area, low dynamic power, and higher speed has made the traditional planar devices susceptible to various sources of variations, thus making these devices unreliable.

According to the International Technology Roadmap for Semiconductors (ITRS) [1], main obstacles that prevent the scaling of planar technology nodes are high leakage power, short-channel effects, gate dielectric leakage and process variations.

To continue with the established trend of technology node scaling and to solve the main problems that the CMOS devices face, various alternative feature structures have been proposed. One of the most promising structures to replace the bulk MOSFET are FinFETs thanks to their stronger gate control, low leakage power, and reduced short-channel effects. Their advantage over bulk MOSFETs has been experimentally demonstrated in [2,3]. In recent years there has been active ongoing research both in academia and industry, and some FinFET based architectures are already being used for volume production.

Although FinFET devices promise to solve some of the major challenges that their planar counterparts face, due to their 3D structure and width quantization, they may introduce new sources of variability. Hence it is crucial to study the performance of FinFET based circuit blocks to identify the key challenges introduced by the new device structures.

The impact of variability on FinFET performance has been studied in the state of the art [4–6]. These studies are all based on the performance of a single type of FinFET model, and at one or more technology nodes.

Typically, and prior to the availability of data about new technologies from the foundries, predictive transistor models are used to explore and model the impact of scaling on device performance, such as threshold voltage, I_{on} , and I_{off} . Such predictive transistor models for FinFET devices are derived either from TCAD simulations [7], or from technology scaling history and early stage silicon data, like Predictive Technology Models (PTM) [6].

In this work, the impact of variability is studied on the performance of digital logic cells, such as NAND and NOR gates. Both PTM and TCAD device models are used and compared with regard to the performance metrics of the logic cells; for example, gate delay. The goal is to provide the reader with an overview of the possibilities of each device model, their similarities and differences, as well as their sensitivity to variations in the process parameter values.

2. Modeling

To identify major variability sources and their impact on FinFET based circuit performance, we base our studies on logic cells. To allow a fair performance comparison between TCAD and PTM transistor model based circuit blocks, each circuit block has to be sized with respect to performance specification and operating conditions based on the respective transistor models. One of the key differences of FinFET transistors compared to planar MOSFETs is the width discretization. This means that transistor sizing in FinFET technology is performed only by changing the number of fins. The key parameters for 14 nm TCAD and PTM models are presented in Table 1.

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Table 1
Key parameters of TCAD and PTM FinFET transistor models.

Parameter	Unit	TCAD	PTM
L_g	nm	20	18
H_{fin}	nm	25	23
T_{fin}	nm	10	10
T_{ox}	nm	0.8	0.75
VDD	V	0.9	0.8

2.1. Discrete sizing

For our study the logic cells have been nominally sized using an automatic discrete nominal sizing algorithm [8]. The objective of the algorithm is to satisfy the performance specification by changing the design parameters (discrete fin numbers). The performance specification (such as delay, transition time, leakage, and dynamic power) is set by upper performance bounds (e.g. maximum delay) and once the gate performance is satisfying all specification bounds, the algorithm terminates.

We base our study logic cells that have been sized using the algorithm described above. The results of discrete nominal sizing for 2-input NAND and NOR cells based on 14 nm FinFET technology are presented in Fig. 1. The logic cells have been sized using both TCAD simulation based and PTM transistor models. Please note, that along with other characteristics TCAD and PTM device models have different nominal channel lengths (18 nm for PTM and 20 nm for TCAD model respectively), as well as different threshold voltage ratios between PMOS and NMOS transistors, hence the sizing objective targeted at the same specification requirement results in different sizings for the two models. On the other hand, we see that the ratio of PMOS/NMOS fin numbers does not follow anymore the conventional sizing ratio of PMOS/NMOS transistors in planar technology.

2.2. Spatial variations

Although FinFETs demonstrate significant performance improvement over planar CMOS, process variations still remain a major challenge in FinFET technology. With increasing divergence between optical wavelengths of lithographic processes and device sizes, the impact of parameter variations on the circuit performance is becoming critical. These variations can be spatially correlated and can be categorized into two main groups: global and local. Parameter variations that affect all the transistors of a die in the same way, are listed as global variations. These can be caused due to a mask offset during the manufacturing process and can affect transistor parameters, such as channel length, width and oxide thickness. On the other hand, Random Dopant Fluctuations (RDF) and Line Edge Roughness (LER) can be categorized as local variations, meaning that they affect two transistors on a same die differently. LER is a result of an imperfect etching process.

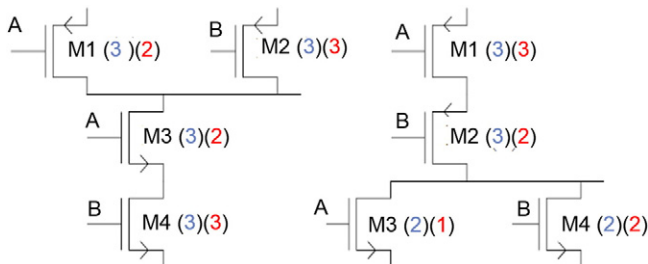


Fig. 1. NAND and NOR cells with corresponding fin numbers for TCAD (blue) and PTM (red) models in parentheses.

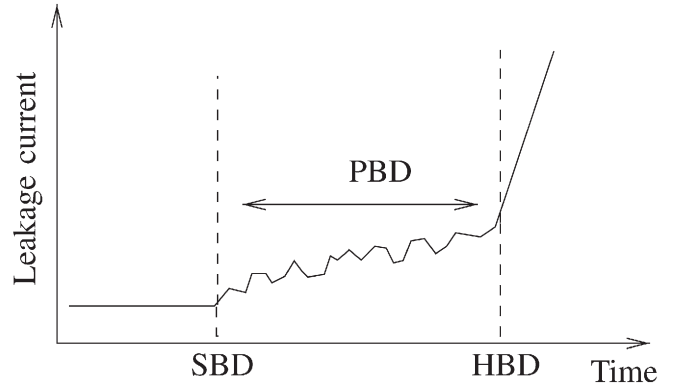


Fig. 2. Evolution of TDDB induced gate leakage current over time.

To evaluate the impact of process variations on circuit performance we assume the global fluctuations of FinFET channel length (L_g), fin height (H_{fin}), as well as fin thickness (T_{fin}) follow a Gaussian distribution. We model the 3σ standard deviations equal to 10% of their nominal values. The global variation of oxide thickness (T_{ox}) is similarly considered to be Gaussian distributed with the 3σ standard deviation equal to the 5% deviation from its nominal value. In addition, we consider also the local variability of T_{fin} and L_g caused by LER.

In older technologies the number of the dopant atoms in the transistor channel was high enough, such that a small fluctuation in the number of atoms would not be catastrophic. However, with shrinking feature sizes the number of dopant atoms in the channel has also decreased, therefore even a small deviation in the number of atoms can have a significant impact on the device performance. RDF causes threshold voltage (V_{th}) variability and for our studies we assume the number of dopants in the channel to be Poisson distributed. The standard deviation due to RDF is given by the following equation [9]:

$$\sigma N_A = \sqrt{\frac{N_A}{L_g \cdot T_{fin} \cdot H_{fin}}} \tag{1}$$

The use of metal as a gate material introduces another important source of FinFET variability. The orientation of the metal grains cannot be controlled during the manufacturing process and as a result these grains will have random orientation. On the other hand, the work function of the gate (ϕ_c) is dependent on the metal grain orientation,

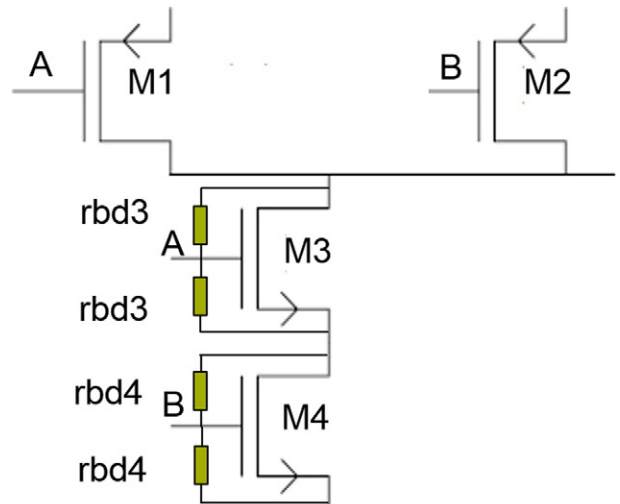


Fig. 3. TDDB equivalent circuit for NAND2.

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