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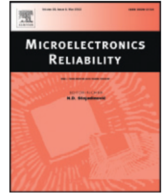

Effects of thermal annealing on the charge localization characteristics of $HfO_2/Au/HfO_2$ stack

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ABSTRACT

To be compatible with the mainstream nano CMOS technology and to further increase the density and to reduce power consumption of non-volatile memory, high-k dielectric will become the major technology option for next generation non-volatile memory technology. To ensure the required retention time and to maintain the scalability of floating gate memory transistor, the charge store in future memory transistor should be accompanied with the high-k insolated metal or conductive clusters, islands, or nano-particles. This work proposes a simple method to fabricate high-k isolated metal cluster array. An $HfO_2/Au/HfO_2$ stack was first grown by using atomic layer deposition (ALD) and thermal evaporation, respectively, for HfO_2 and Au film deposition. After a high-temperature thermal annealing, a number of HfO_2-buried Au islands with diameter of about 5 to10 nm were obtained. Capacitance–voltage (C–V) measurements show that the charge storage characteristics of the Au-embedded HfO_2 structure were affected greatly by the annealing conditions. Depending on the annealing temperature (it should be governed by thickness of Au layer also), the thermal annealing may lead to the formation of Au islands/clusters, the improvement of HfO_2 blocking property as a result of defect removal, or the deterioration of the blocking property of HfO_2 due to the crystallization of HfO_2 film. Process optimization should be conducted for further improving the charge localization characteristics.

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1. Introduction

Driven by further CMOS device downsizing and the continuous improvement in metal gate/high-k technology, high-k based memory technology has attracted much attention recently [1–5]. High-k has been the only way for achieving subnanometer equivalent oxide thickness (EOT) gate dielectric film for decananometer MOS devices [6–7]. The use of high-k film also benefits the memory devices such as flash memory in several ways. High-k dielectrics have smaller band offsets in both conduction band and valence band [6]; it enables the memory transistors be operated at lower "write" and "erase" voltages than that of conventional silicon dioxide and new kinds of programming mechanisms will be possible due to the availability of bipolar charge injection and depopulation [4]. During read mode or off mode, in principle, the memory content should be able to keep for longer duration as the physical thickness of the high-k dielectric should be much larger than the ultrathin tunneling silicon oxide used in the current commercial products. Meanwhile, the flash memory technology based on the floating gate memory transistor now also comes across with several issues resulted from the device downsizing. The tunneling oxide is now much thinner, the transistor size and power dissipation per cell should also be much smaller so as to increase the storage density. This trend makes the reliability of the memory transistor be more vulnerable to a single oxide defect. A feasible solution to these issues is the replacement of the single floating gate with a number of isolated floating islands [8–12]. This technique should also be a must recipe for high-k based memory transistors. It is the promising way to meet the 10-year retention time as specified for non-volatile memory devices and the required process variability also for high-k based memory devices [1]. Various candidates of nano-particles including Si nano-particles and metal nano-particles have been studied [12–14]. Amongst the various high-k dielectrics being studied, HfO_2 has already been used in the most advanced IC manufacturing [15–16]. It is a mature technological option now not to mention that HfO_2 has many superior properties than other high-k materials [16–17]. Several attempts have been made [2,9,14]. However, HfO_2 and other high-k dielectrics are found to have much higher bulk defect density than that of conventional materials [15–17]. Charge loss due to the trap-assisted current conduction can degrade the retention time significantly [2].

The objective of this work is to investigate the effect of thermal annealing on the electrical characteristics of HfO_2-isolated Au islands which was obtained by high-temperature annealing on a $HfO_2/Au/HfO_2$ sandwich structure. Flatband voltage shifts under different voltages and

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from differently annealed samples that were analyzed in detail to study charge localization characteristics of the structure.

2. Experiment

Fig. 1 shows the schematic cross-sectional views of the HfO_2/Au/HfO_2 stack with and without thermal annealing. The starting material was <100> orientated n-type silicon wafer with resistivity in the range of 1–10 Ω-cm. After standard cleaning, the wafer was immersed in hydrofluoric acid solution to remove the native oxide. A 5 nm thick HfO_2 was first deposited by atomic layer deposition (ALD) at 270 °C by using $Hf[(CH_3)_2N]_4$ and water vapor as the precursors. An Au layer of about 2 nm thick was then deposited with e-beam evaporation. Next, another layer of HfO_2, of 5 nm thick also, was deposited with the same ALD process to cover the Au layer. The as-deposited HfO_2/Au/HfO_2 stack was then annealed in N_2 ambient at temperature ranging from 550 to 800 °C for 30 min or 60 min. The structural changes after the thermal annealing were examined with high-resolution cross-sectional transmission electron microscopy (TEM) measurements. A 60 nm thick Au layer together with a 5 nm thick Cr buffer layer was then deposited by e-beam evaporation. Finally, a number of metal electrodes with a diameter of 200 μm, used for the purpose of electrical measurements, were patterned. To study the charge storage characteristics of the HfO_2-isolation Au islands, bi-directional capacitance–voltage (C–V) measurements were conducted on various samples after different thermal treatments with Agilent B1500A semiconductor characterization system. All the measurements were done at room temperature.

3. Results and discussion

Fig. 2 shows some typical cross-sectional views with increasing magnification factor, of the sample after thermal annealing at 800 °C.

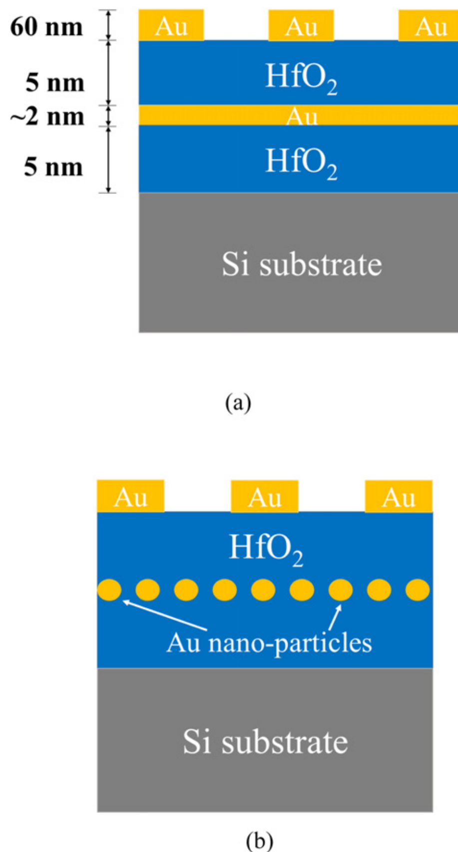

Fig. 1. Schematic showing the cross-sectional views of the Au/HfO_2/Au/HfO_2/Si structure before thermal annealing (a), and after thermal annealing (b).

The fine structure in Fig. 2(d) shows that the Au layer was converted into some small clusters/islands, well encapsulated with HfO_2 insulating layer, with diameters in the range of 5 to 10 nm. These conductive islands serve as charge storages with improved retention time for memory devices. Fig. 3 shows a typical high-frequency (1 MHz) C–V curve. C–V hysteresis can be seen by conducting a bi-directional voltage scan [16]. During the forward scanning (from negative voltage to positive voltage), electrons are injected into the dielectric film and some of them may be captured at the trap sites in the dielectric film. The trapping of electrons causes a positive shift in the C–V curve. During the backward scanning, some of the trapped charge may be depopulated and gives rise to a negative shift in the C–V curve. This C–V hysteresis will be enhanced for metal incorporated dielectric film as a result of charge localization in the metal cluster sites, which is the working principle for using metal-embedded high-k dielectrics as memory devices. Unfortunately, high-k materials were found to have higher defect density and have larger leakage current [17]. Charge trapping activities at defect sites are less controllable. The wide range of energy distribution of the defects made the charge depopulation events unpredictable. In addition, the retention time will be significantly shortened due to the large leakage current of the dielectric film. In this work, we study the effects of thermal annealing on the charge localization effects by monitoring the voltage shift in C–V measurements.

Fig. 4 depicts the flatband voltage shift as a function of annealing temperature. Here, each data point represents an averaged value of those extracted from six C–V measurements on different devices on the same wafer. As depicted in Fig. 4(a), the voltage shift almost increases linearly with the annealing temperature for annealing temperature lower than 750 °C. This observation can be attributed to the improved blocking property of the HfO_2 film. It was reported that the as-deposited HfO_2 films were often found to have large leakage current because of the defects, especially the oxygen vacancies and water-related trap centers [15–16]. Thermal annealing at temperature lower than 750 °C can improve the film characteristics significantly [15–16]. This trend was also found in this work. Fig. 4(b) depicts the annealing effect on sample without Au layer. As temperature increases, the flatband shift becomes smaller as a result of defect density reduction in the film. Because of the lower defect density and then the smaller leakage current of the annealed samples, the injected charge can be better stored in the Au layer and then a large voltage shift in C–V hysteresis of the Au samples emerged (see Fig. 4(a)). However, for samples annealed at 750 °C and above, a sharp drop in the voltage shift was found for sample with Au islands. This trend should be due to two consequences related to high-temperature annealing. First, we found for the 2 nm thick Au film embedded in HfO_2 that the film still remains to continue after annealing at a temperature lower than 750 °C. It was broken into some small clusters or islands if the temperature is at 750 °C or above. Some Au atoms are lost during this process. That means the charge storage capability will be reduced under this situation although the "island form" of metal can improve the retention time significantly. Second, it was reported that HfO_2 films are easy to have local crystallization for high-temperature (e.g. >700 °C) annealing [17]. The grain boundaries of micro/nanocrystallites of the HfO_2 can serve as shallow traps which assist in the current conduction [17–19]. That means the blocking capability of HfO_2 film will be degraded if there exists some crystallites. Hence, the higher temperature annealing (750 °C and above) would result in the reduction of both charge store capability of Au film and blocking capability of HfO_2 and that a sharp drop in the voltage shift in Fig. 4(a) resulted. Nevertheless, this work demonstrates a simple way to form metal clusters embedded high-k film. Yet thinner metal film should be used so that the clusters can be formed at lower annealing temperature to eliminate the crystallization effect of the high-k film. It calls for better facilities for ultrathin metal film deposition and some additional process optimization effort also.

Fig. 5 shows the C–V voltage shift for the Au/HfO_2/Au/HfO_2/Si structure biased at different "program voltages". The HfO_2/Au/HfO_2 stack was

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