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Impact of temperature on linearity and harmonic distortion characteristics of underlapped FinFET

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ABSTRACT

In this paper, the performance of asymmetric underlapped FinFETs (U-FinFETs) is analyzed for linearity and harmonic distortion at high temperatures. The harmonic distortion that arises as a result of non-linear device characteristics requires a detailed analysis for better RF reliability performance. The variations in linearity and distortion characteristics with temperature are analyzed with regards to the primary components of harmonic distortion, second order distortion (*HD2*), third order distortion (*HD3*), and the total harmonic distortion (*THD*). For detailed understanding of the distortion characteristics of U-FinFETs, different device parameters such as the drain current (I_{ds}) and transconductance (g_m) are also analyzed. The results of the analysis suggest that the U-FinFETs present a significant reduction in harmonic distortion at elevated temperatures under subthreshold regime and restrict the degradation in harmonic distortion in the superthreshold regime resulting in better reliability for RF applications.

1. Introduction

The advancement in CMOS technology has significantly increased the analog and RF circuit design activities for the system on chip (SOC) applications. The CMOS technology has evolved owing to various performance enhancing structural modifications of the conventional MOSFET structure. Presently, the double gate MOSFET (DG-MOSFET) architecture has been constituted to provide superior analog/RF performance [1–3]. However, due to higher short channel effects (SCEs) this device suffers from degraded gate control under high drain to source voltage (V_{ds}) [3]. Thus, the DG-MOSFET structure is modified by introducing an underlap to isolate both the source and drain namely, the symmetric underlap DG-MOSFET (SUDG-MOSFET), to overcome the detrimental effects of SCEs [4–10]. However, the source/drain (S/D) underlap reduces the on current (I_{on}) of the devices in comparison to the conventional overlap DG-MOSFET. Thus, it is more efficient to use only drain side underlap for an optimized SCE and I_{on} [11]. So, in this work the asymmetric underlap FinFET (U-FinFET) device is analyzed and compared to FinFETs for reliable analog and RF performances.

Although the device performance is significantly improved, the on chip performance of the device is subject to various external factors such as operating temperature. With increasing number of on-chip transistors the total amount of heat dissipation significantly increases; as a result the operating temperature also increases. Thus, it is important to pre-emptively analyze the impact of temperature on device performance for better reliability. In previous works, the impact of temperature on silicon on insulator (SOI) MOSFET devices like FinFETs has been studied extensively for digital and analog applications [12,13]. However, for reliable analog and RF circuit design it is crucial to estimate the impact of temperature on the inherent reliability issues such as the linearity and the harmonic distortion (HD) of the CMOS devices [14,15].

In this paper, a detailed analysis of the distortion characteristic of U-FinFETs due to the non-linear nature of the drain current (I_{ds}) is presented as a function of increasing operating temperature. The device structure and the simulation procedure for this analysis are presented in Section 1, followed by the linearity analysis in Section 3. In Section 4, HD analysis of the devices is addressed and finally, the conclusion is presented in Section 5.

2. Device structure & simulation

The specifications of the U-FinFET structure analyzed are illustrated in Fig. 1. The device structure is described by the silicon body thickness (t_{si}) of 16 nm, the gate length (L_{gate}) of 45 nm with an oxide thickness (T_{ox}) of 1.9 nm and a drain side underlap [11]. The source/drain (S/D) lengths are 50 nm. The drain to gate underlap length (L_{un}) is considered to be 20 nm after optimization, as described in [11]. The n^+ S/D doping of the device is 10^{20} cm^{-3} and the silicon body is lightly doped with doping concentration of 10^{15} cm^{-3}.

The U-FinFET device presented in Fig. 1 is simulated with the three-dimensional (3D) numerical device simulator Sentaurus [16] and for accuracy and robustness the meshing strategy is optimized as described in [17]. In the device simulation, density-gradient model is used for carrier

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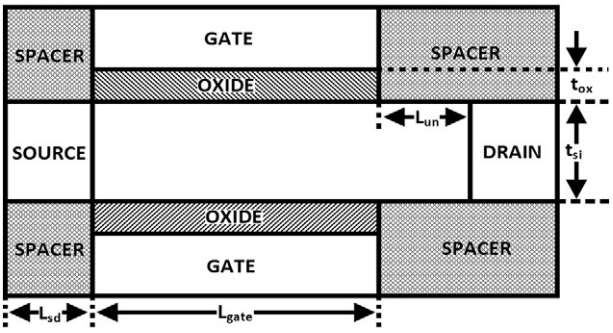

Fig. 1. Cross section of an idealized underlap FinFET (U-FinFET) with drain side underlap.

transport. The active carrier lifetime and density is dictated by the Shockley–Read–Hall (SRH) recombination and the incomplete ionization models, respectively. The mobility degradation including ionized impurity scattering is accounted by using the Lombardi mobility model. The calibration of the simulator as presented in Fig. 2 is done with the experimental data [18] considering the carrier mobility as described in [19]. The field dependence of mobility is calibrated by using Enormal with Lombardi model parameters and the doping dependence is calibrated by adjusting the Aurora mobility model parameters. The simulated device is used to extract the I_{ds}–V_{gs} characteristics at different ambient temperatures as shown in Fig. 3 where, V_{gs} is the gate to source voltage. Subsequently, the I_{ds}–V_{gs} characteristics data are used for extracting and analyzing the distortion characteristics.

In the study, the distortion characteristics are extracted by implementing the Integral function method (IFM) [20]. In the IFM, the deviation of the non-linear characteristics from the linear one is represented by different integral functions.

For linearity analysis of the device, the third order intercept point (IIP_3) is considered. For harmonic distortion, the impact of temperature is studied on distortion figure of merits (FOMs), the total harmonic distortion (*THD*), second order harmonic distortion (*HD2*), and the third order harmonic distortion (*HD3*) introduced by the device.

3. Linearity analysis

An important aspect for an analog/RF circuit design using CMOS technology is to ensure minimum intermodulation and higher-order harmonics at the output. Also, the HD of a circuit is important because the device non-linearity should be nominal. However, the non-linear characteristics of the device vary with increasing operating temperature

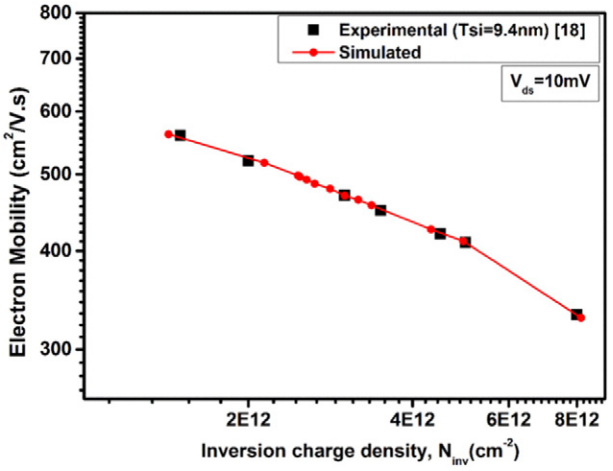

Fig. 2. Calibration of electron mobility with experimental results [18] as a function of inversion charge density.

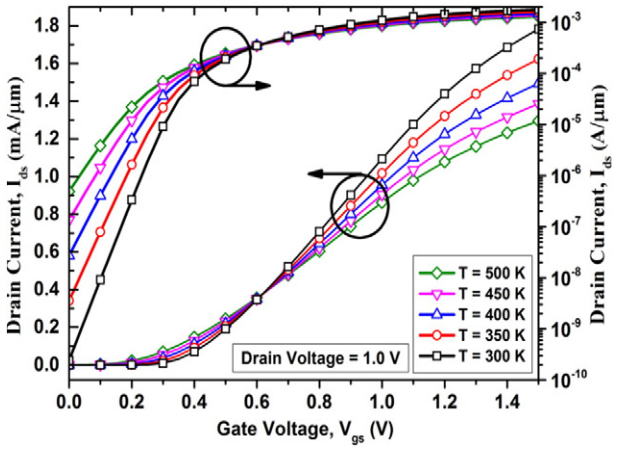

Fig. 3. The drain current (I_{ds}) of U-FinFETs as a function of gate voltage, V_{gs} for increasing operating temperature, T.

posing a reliability concern. In this study, the linearity of the device is evaluated as a function of the intercept point between the fundamental frequency and the third harmonic output power defined as IIP_3 [21–23]. The IIP_3 of a device is inversely proportional to third order derivative of I_{ds} [21]. The variation in IIP_3 at the point of maximum g_m for U-FinFETs with increasing operating temperature is presented in Fig. 4.

It is observed from Fig. 4 that the linearity of U-FinFETs is significantly higher than that of FinFETs. It is also observed that the linearity of U-FinFETs decrease with increasing operating temperature in contrast to FinFETs. For FinFETs the linearity increase with temperature is attributed to higher influence of drain bias [24]. This is because the higher drain bias induces early onset of surface roughness scattering dependent mobility which is weakly dependent on temperature [25]. This drain bias dependence is briefly discussed in the following section.

For U-FinFETs, although the linearity degrades with temperature, the degradation is noticeably low standing at 1.4 dBm for an about 200 K temperature change. This slight degradation in the linearity of U-FinFETs can be elucidated from the g_m–I_{ds} plot presented in Fig. 5.

It is observed in Fig. 5 that the flattening of the g_m–I_{ds} characteristics decreases with increasing temperature resulting in higher value for third order derivative of I_{ds} thereby, degrading the linearity of the device [21]. The reduced flattening at higher temperatures is physically attributed to a rapid reduction in g_m with I_{ds} due to enhanced lattice vibration induced carrier scattering. However, due to the presence of non-

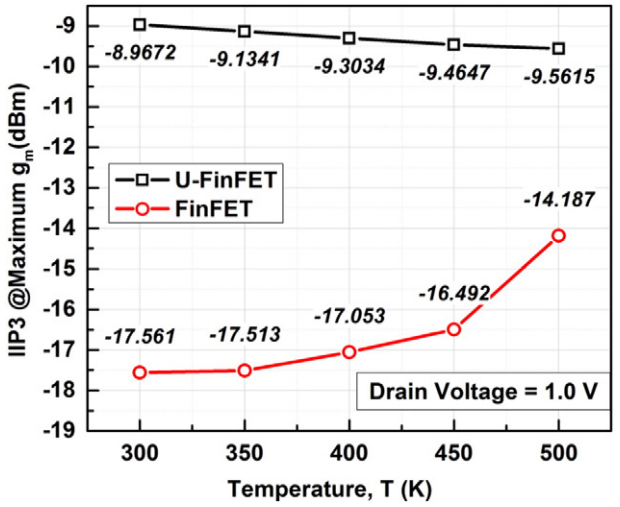

Fig. 4. Variation in the third order output power point of intercept, IP_3 for U-FinFETs and FinFETs at maximum g_m point as a function of operating temperature, T.