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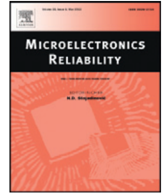

Very small snapback silicon-controlled rectifier for electrostatic discharge protection in 28 nm processing

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ABSTRACT

A novel silicon-controlled rectifier (SCR)-based device with very small snapback is proposed in this paper. New features including an embedded gate-to-VDD PMOS (GDPMOS) and lateral n-p-n BJT are used to achieve low trigger and high holding voltages suitable for electrostatic discharge (ESD) protection of 28-nm CMOS technology with very narrow ESD operation windows. Measured results show an ESD operation window of less than 1 V. TCAD simulation is also carried out to demonstrate the underlying physical mechanisms.

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1. Introduction

With the continuously scaled down CMOS process, electrostatic discharge (ESD) induced damages have become a serious reliability issue [1]–[2]. In the advanced CMOS processes, such as the 28-nm technology node, the trigger voltage of ESD protection devices must be relatively low due to the thin gate oxide, and the holding voltage must be relatively high to mitigate the risk of latch-up. With a 10% safety margin, the ESD design window should be between 0.9 × TBV (transient gate break down voltage) and 1.1 × VDD. For the 28-nm process, a typical ESD design window in *I/O* pins is 2.8–8.4 V.

Silicon-controlled rectifier (SCR) is well known for its high robustness, however the SCR has the drawbacks of relatively low holding voltage and high trigger voltage [3]. Modified methods have been reported to resolve this problem [4–7]. For example, the high-holding-voltage SCR (HHVSCR) was proposed in [8–10]. By inserting a P-drift region and a second N-well in the SCR, the holding and trigger voltages of the HHVSCR are around 5 V and 9 V, respectively. But such a snapback is still too large to satisfy the ESD design window requirement of the 28-nm CMOS process.

In this letter, a novel SCR with small snapback (SSSCR) realized in the 28-nm CMOS process is proposed for effective and robust ESD protection applications. Measurement results obtained from the transmission line pulsing (TLP) tester are used to validate the device performance, and TCAD simulation is carried out to share the insight of device's behavior under the ESD stress condition.

2. Results and discussion

2.1. HHVSCR

The cross-sectional views of the conventional SCR and HHVSCR structures fabricated in the 28-nm CMOS process are shown in Fig. 1(a) and (b), respectively. By inserting a P-drift region and a second N-well in the SCR, HHVSCR is formed [10].

The holding voltage varies with design parameters. *D1* is the length of P-drift region in P-well, and *D2* is the length of P-drift region in the second N-well. As can be seen from Fig. 2, the holding voltage increases with *D1* increasing. The holding voltage of HHVSCR increases from 5.3 to 7.3 V when *D1* changes from 2 to 4 μm. It is mainly caused by the increase of ESD current path between anode and cathode. Fig. 3 shows the TLP testing results with three different *D2* values. It is clear that *D2* has less effect on the holding voltage than *D1*.

However, the trigger voltage is nearly 9 V, it is too high for the weak gate of the 28-nm CMOS process. Therefore, a new structure is needed to protect the device in 28-nm process. SSSCR is proposed and analyzed in the following section.

2.2. SSSCR

The cross-sectional view of SSSCR structure is shown in Fig. 1(c). The SSSCR differs from the conventional SCR in the following two main aspects. A gate is placed above the N-well and connected to the anode [4], and a second N-well is added and is interfaced to the P-well. Fig. 4 compares the TLP *I-V* curves measured from the SSSCR, HHVSCR, and conventional SCR having the same device width of 30 μm. The ESD performances of these devices are also summarized in Table 1. These

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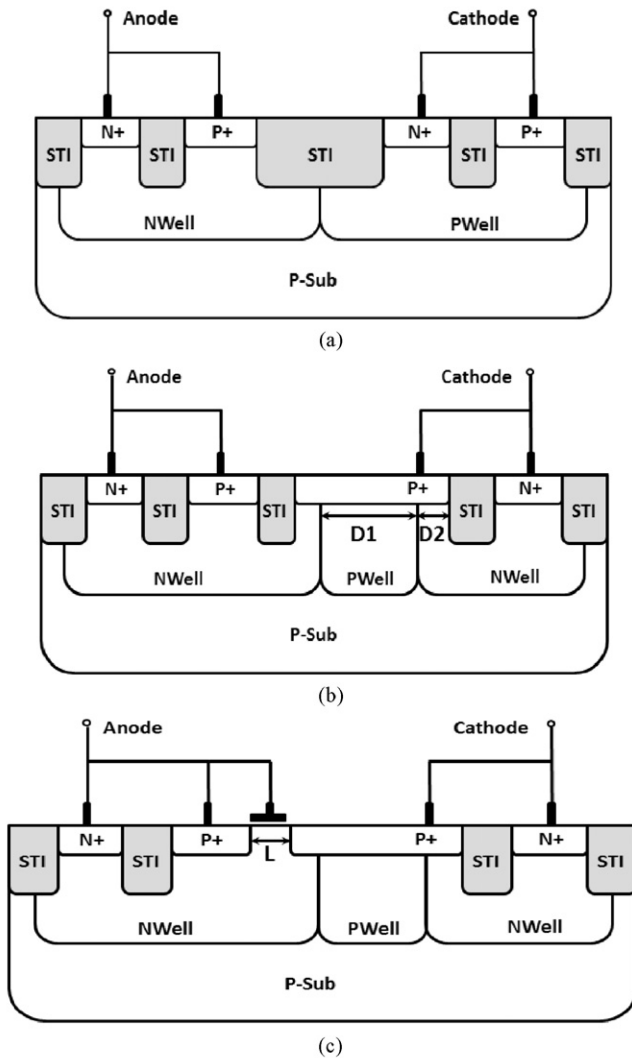

Fig. 1. Cross-sectional views of the (a) conventional SCR, (b) HHVSCR and (c) SSSCR structures.

structures have a similar normalized failure current of 43.3 mA/μm and leakage currents at the nano-ampere level. For comparison, the normalized failure current of the PMOS device with embedded SCR proposed in [7] is 28.6 mA/μm. Among these three devices, only the SSSCR meets the ESD design window requirement for the 28-nm process. The conventional SCR possesses a trigger voltage higher than the upper limit of the ESD design window. It is because the triggering in these devices requires the avalanche breakdown of the N-well/P-well junction. For the SSSCR and HHVSCR, however, the triggering takes place at the N-well/P+ junction, resulting in a smaller trigger voltage. The added gate structure can induce the halo implants which consequently reduce the trigger voltage further because the concentration of halo implants is higher than that of N-well.

The channel length L of SSSCR is a key parameter that can be varied to change the holding voltage. Fig. 5 shows the TLP testing results with three different L values. As can be seen clearly from the inset of Fig. 5, the trigger voltage is insensitive to L, but the holding voltage increases with L decreasing. The holding voltage of SSSCR increases from 5.3 to 6.5 V when L changes from 1 to 0.15 μm. Therefore, shrinking L can not only save silicon area, but also increase the holding voltage. Note that the SSSCR with $L = 0.15$ μm has a very small ESD operation window of less than 1 V.

In order to explain the underlying physical mechanism of the effect of L on the holding voltage, Fig. 6 is given to show the TCAD simulation results. Fig. 6(a) depicts the current density contours at an anode current of 10 mA with $L = 0.5$ μm, which indicates that the initial flow of current in the SSSCR is through the P+-to-N-well-to-P+ (P-drift) path. In this case, the ESD stress is released via the embedded GDPMOS. Fig. 6(b) shows the current density contours at the same anode current with $L = 1$ μm. It can be found that the current flows further away from the silicon surface when the channel length is increased. As a result, a large portion of current is routed through the P+-to-N-well-to-P-well-to-P+ (P-drift) path. This increases the potential of P-well, and finally the P-sub-N-well (the second N-well) diode becomes forward biased, leading to the turn-on of the lateral N-well-P-sub-N-well (NPN bipolar). Therefore, increasing in the channel length turns on the SCR path earlier and hence gives rise to a smaller holding voltage.

The *I-V* characteristic of SSSCR has also been measured with different temperatures to investigate temperature dependence of the holding

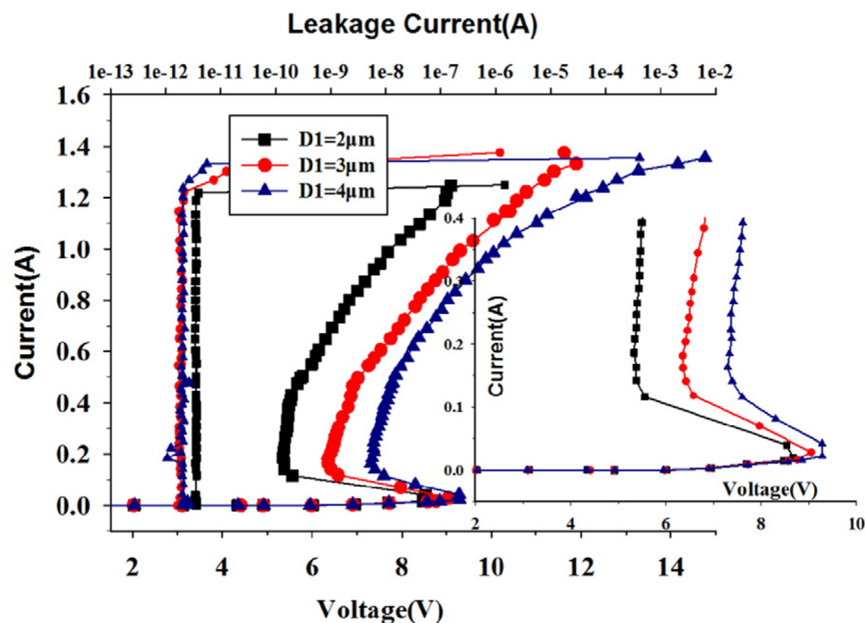

Fig. 2. TLP *I-V* data measured from the HHVSCR having three different *D1* values.

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