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Comparative study of reliability degradation behaviors of LDMOS and LDMOS-SCR ESD protection devices

Zhihui Yu [a], Hao Jin [a,*], Shurong Dong [a], Hei Wong [b], Jie Zeng [a], Weihuai Wang [a]

[a] Department of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China
[b] Department of Electronic Engineering, City University of Hong Kong, Hong Kong

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ABSTRACT

This paper presents a comparative study on the electrostatic discharge (ESD) characteristics of Lateral Diffused Metal-Oxide-Semiconductor (LDMOS) and LDMOS with embedded silicon controlled rectifier (LDMOS-SCR) by using transmission line pulsing (TLP) measurements. Results show that the safe operating area (SOA) of LDMOS shrank pronouncedly and its reliability degraded due to the walk-in of trigger voltage (V_{t1}). The V_{t1} walk-in is attributed to the so called weak spot filament created/grown near the N+ drain region in previous ESD strike. The isolation drain structure in LDMOS-SCR can solve this issue. However, both devices were found to be not robust enough when they were subjected to be operated at high temperature ambient.

1. Introduction

High-voltage (HV) devices are widely used in smart-power integrated circuits, such as automotive electronics, high-voltage circuit drivers, and power management circuits. Same as low-voltage CMOS process, electrostatic discharge (ESD) reliability has become one of the critical issues in HV devices [1–2]. It was found that in some situations, the HV devices themselves are not capable be self-protected against the ESD stress, additional ESD protection devices are still required. Laterally-diffused metal-oxide-semiconductor (LDMOS) and LDMOS with embedded silicon control rectifier (LDMOS-SCR) are proposed for providing ESD protection in HV process [3–5]. In short, the inherent parasitic bipolar junction transistor (BJT) or the embedded SCR of the LDMOS which provides additional current path serves as the key mechanism for ESD protection. However, these devices were also found to be degraded gradually when they are subjected to multiple ESD strikes. By applying ESD strike on LDMOS repeatedly, the trigger voltage (V_{t1}) will decrease progressively and this degradation becomes severer with the presence of gate bias [6–7]. In addition, trigger voltage of LDMOS-SCR is also found to be governed by the operation temperature. The leakage current increases sharply as the temperature rises. These degradation phenomena may give rise to mis-triggering and increase the power dissipation of devices. This paper presents a comparative study on the ESD reliability degradation of LDMOS and LDMOS-SCR at different temperatures.

2. Device structures and experimental results

Fig. 1 shows the cross-section view of an N-type LDMOS and LDMOS-SCR. Conventional LDMOS and LDMOS-SCR have been fabricated in 0.35 μm 40 V BCD process (W = 40 μm). For ESD characterization, I–V curves are measured by 4002 Barth TLP system with the pulse width of 100 ns and a rise time of 10 ns.

In the LDMOS structure given in Fig. 1(a), the N+ implant in the N_{DD} layer, P-body, and N+ implant in P-body constitutes the parasitic BJT of the LDMOS. When the drain-to-source is sufficiently large, i.e. with an ESD strike, the HV N-well/P-body junction will be broken down. Under this situation, the parasitic BJT turns on and a snapback of current–voltage characteristic occurs. As shown in Fig. 2(a), the trigger voltage of the first TLP strike is 68.7 V. Different from conventional TLP test that TLP zapping on the device was applied till second breakdown point (i.e. failure point), our ESD strike stopped at snapback which is far before the failure point. A second ESD strike was then applied and we found that the trigger voltage now degraded to 50.3 V. This degradation phenomenon is called walk-in effect [6]. The trigger voltage walk-in behavior imposed some constraints for ESD protection device designs. The walk-in phenomenon can be enhanced with a gate bias and the rise of the operation temperature. As shown in Fig. 3(a), the second trigger voltage (ΔV_{t1}) increases from 18.4 V to 20.0 V when the temperature rises from 25 °C to 100 °C. It becomes severer with the presence of gate bias. As shown in Fig. 3(b), trigger voltage is 50.3 V when the gate is grounded; it reduces to 37.2 V for a 0.5 V gate bias. These results can be ascribed to the charge accumulation on the gate oxide which can be enhanced with a gate bias.

* Corresponding author.
E-mail address: hjin@zju.edu.cn (H. Jin).

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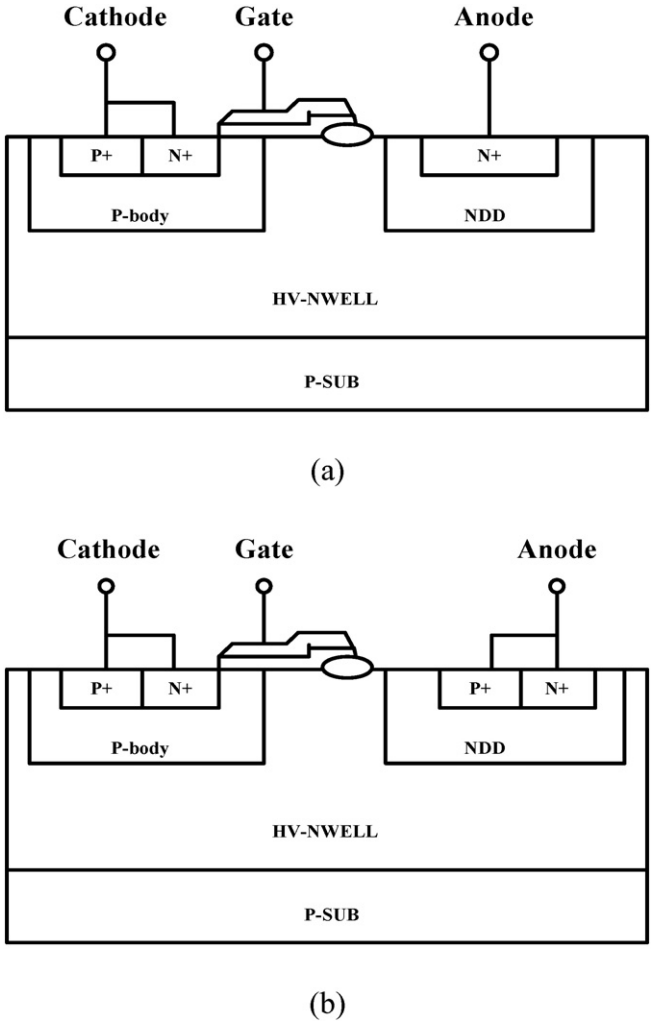

Fig. 1. Cross-section view of (a) LDMOS and (b) LDMOS-SCR realized with a 40 V 0.35 μm BCD process.

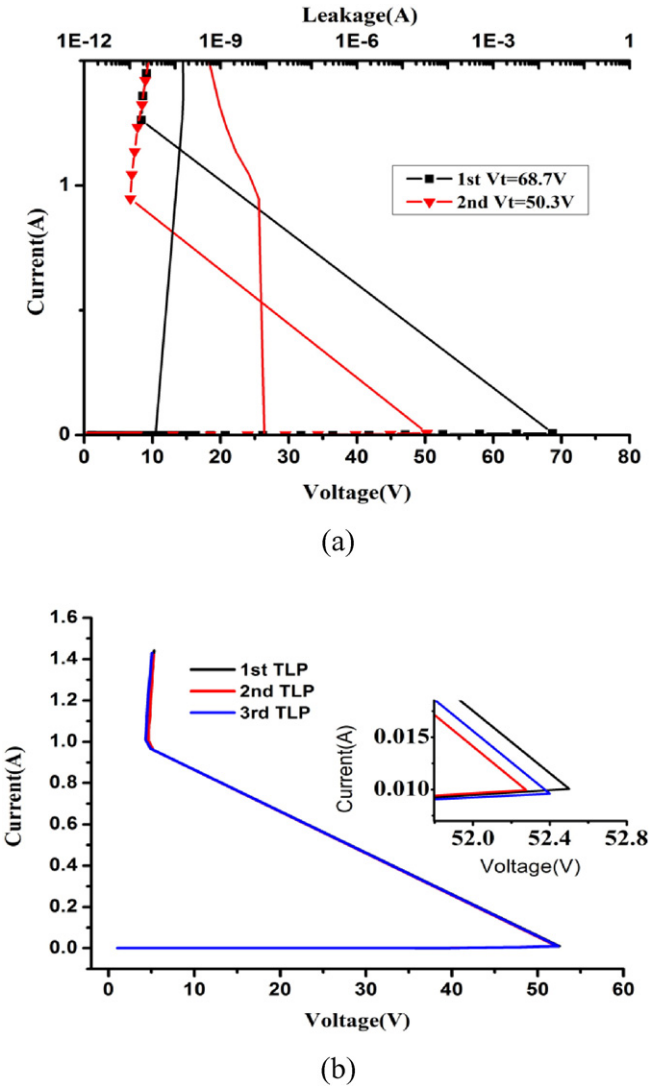

Fig. 2. (a) Results of TLP strikes on LDMOS. Trigger voltage walk-in is found during the second ESD zap. (b) Results from LDMOS-SCR clamp show a negligible walk-in effect for the trigger voltage.

For the LDMOS-SCR case, the parasitic SCR is constituted by the P+ implantation beside N+ drain region of LDMOS (see Fig. 1(b)). When an avalanche breakdown occurs in the LDMOS, the generated holes flow through R_p (parasitic resistance in P-body) and are collected in the P+ region of source. When the voltage drop across R_p exceeds 0.7 V, the parasitic NPN bipolar will be turned on. As a result, the current across R_n (parasitic resistance in N-well) increases which in turn makes the PNP bipolar to be turned on. After this, the intrinsic regenerative feedback mechanism between parasitic PNP and NPN generates and the device begins to discharge heavy current. Again, the LDMOS-SCR also experiences trigger voltage degradation at high temperatures. As shown in Fig. 4(a), V_{t1} even becomes smaller than the working voltage. Although the LDMOS-SCR structure has a less walk-in effect as compared with the LDMOS ones, the trigger voltage still degrades in high temperature. As shown in Fig. 4, the trigger voltages are 52.4, 44.0, and 35.6 V, respectively, in 25, 100, and 150 °C. In particular, the trigger voltage at high temperatures is lower than the working voltage. That is LDMOS-SCR can be turned on even without ESD event. On the contrary, the trigger voltage of LDMOS almost remains unchanged at different temperatures.

3. Discussion

The unstable trigger voltage makes the SOA to be shrunk and impose a number of challenges for ESD protection design. In the present study, we found that the trigger voltage of LDMOS-SCR device almost remains unchanged (see Fig. 2(b)). At this point, LDMOS-SCR should be much better. The trigger voltage walk-in in LDMOS is attributed to the growth of melt filament region in the N+ drain when an avalanche breakdown occurs [8]. After the first ESD strike, the high field region between the base and collector of the parasitic BJT moves toward the highly-doped collector region. Thus, once the parasitic BJT in the LDMOS is turned on, large heat will dissipate near the N+ drain region and that become a weak spot which can be melted more easily as similar to the breakdown of a filament if more heat accumulates. Since the ESD strike is stopped before the melted down or permanent failure, the LDMOS can still function in the next ESD strike but its trigger voltage is degraded now. Unlike LDMOS, the N+ drain in LDMOS-SCR structure is isolated with the embedded P+ implantation, the excessive current conduction path mainly via the parasitic SCR and the forming weak spot region can be avoided.