Microelectronics Reliability 61 (2016) 115–119

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Design and optimization of LDMOS-SCR devices with improved ESD protection performance

Hailian Liang [a], Huafeng Cao [a], Xiaofeng Gu [a,*], Zixiang Guo [b]

[a] Engineering Research Center of IoT Technology Applications (Ministry of Education), Department of Electronic Engineering, Jiangnan University, Wuxi 214122, China
[b] School of Earth and Space Sciences, University of Science and Technology of China, Hefei 230026, China

ARTICLE INFO

Article history:
Received 15 September 2015
Received in revised form 6 January 2016
Accepted 2 February 2016
Available online 10 February 2016

Keywords:
Electrostatic discharge (ESD)
Lateral diffusion metal-oxide semiconductor embedded silicon controlled rectifier (LDMOS-SCR)
Optimization

ABSTRACT

The lateral diffusion metal-oxide semiconductor embedded silicon controlled rectifier (LDMOS-SCR) devices with optimized structures and layouts for improving the electrostatic discharge (ESD) protection ability have been proposed. The devices are designed and fabricated in 0.25-μm, 0.35-μm and 0.5-μm Bipolar-CMOS-DMOS processes. Firstly, by designing an appropriate stripe resistance in series with the source of the LDMOS-SCR, the holding voltage of the proposed high resistance LDMOS-SCR (HRLDMOS-SCR) increases. Secondly, by inserting a floating Zener-diode into the LDMOS-SCR, the trigger voltage of the modified Zener-diode triggered LDMOS-SCR (ZTLDMOS-SCR) decreases. Finally, the ZTLDMOS-SCR is further optimized by using a ring layout and incorporating a square source resistance, resulting in a significantly improved figure of merit in comparison to traditional LDMOS-SCR devices. The optimized ZTLDMOS-SCR devices are very attractive for constructing effective and latch-up immune high voltage ESD protection solutions in power integrated circuits.

1. Introduction

With the rapid development of power integrated technology, power integrated circuits (PICs) have been widely applied to consumer and automotive electronics [1], making them smaller and cost-effective. However, portable electronics are more susceptible to failure resulting from electrostatic discharge (ESD) during transportation and usage. High voltage (HV) ESD protection design in PICs has become one of the most severe reliability issues due to the large operating voltages and small silicon area [2].

In general, the desired characteristics of high voltage (HV) ESD protection devices are strong robustness and high holding voltage (V_h). Lateral diffusion metal-oxide semiconductor (LDMOS) is a promising ESD protection device due to its low turn-on resistance and good compatibility with commercial CMOS processes [3]. However, its practical applications are usually limited by the small unit area ESD robustness. The silicon controlled rectifier (SCR) [4], the LDMOS-embedded SCR (LDMOS-SCR) [5] and the insulated gate bipolar transistor (IGBT) [6] are attractive ESD protection devices due to their strong robustness, but all of them possess latch-up risks resulting from their low V_h. Although the LDMOS-SCR source engineering reported by Ker et al. [7] can increase the V_h, other characteristics of the ESD performance such as failure current (I_{t2}) and area efficiency need further improvement. A figure of merit (*FOM*) that incorporates all of these parameters is defined as $V_h \times I_{t2}/(V_{t1} \times S)$ [8–9], where V_{t1} and S are the trigger voltage and device area, respectively. Although the waffle layout design of LDMOS reported by Han et al. [10] was useful for increasing the I_{t2}, the trade-off between a high V_h and a large *FOM* still requires further investigation.

In this paper, LDMOS-SCR based devices with optimized structures and layouts have been designed and fabricated in various Bipolar-CMOS-DMOS (BCD) processes. By connecting an appropriate stripe resistance with the source of the LDMOS-SCR and naming the proposed device as the high-resistance LDMOS-SCR (HRLDMOS-SCR), the V_h increases largely in comparison to the standard LDMOS-SCR. By inserting a floating Zener-diode formed by the highly implanted n+ and p+ regions in the LDMOS-SCR and naming the modified device as the Zener-diode triggered LDMOS-SCR (ZTLDMOS-SCR), the V_{t1} decreases significantly. This ZTLDMOS-SCR can be further optimized by using a ring layout and connecting a square resistance with its source. The V_h and *FOM* of the optimized ZTLDMOS-SCR can be increased significantly, making it suitable for constructing effective and latch-up immune HV ESD protection solutions for PICs.

2. Structural description of devices

The cross sections of the LDMOS-SCR, HRLDMOS-SCR, ZTLDMOS-SCR are shown in Fig. 1(a), (b) and (c), respectively. Compared to the LDMOS-SCR, the cathode of the HRLDMOS-SCR is not connected directly with its source and gate, helping to increase the V_h by increasing the current path and the turn-on resistance. Compared to the LDMOS-SCR

* Corresponding author at: Department of Electronic Engineering, Jiangnan University, 1800 Lihu Avenue, Wuxi, Jiangsu 214122, China.
E-mail address: xgu@jiangnan.edu.cn (X. Gu).

http://dx.doi.org/10.1016/j.microrel.2016.02.001
0026-2714/

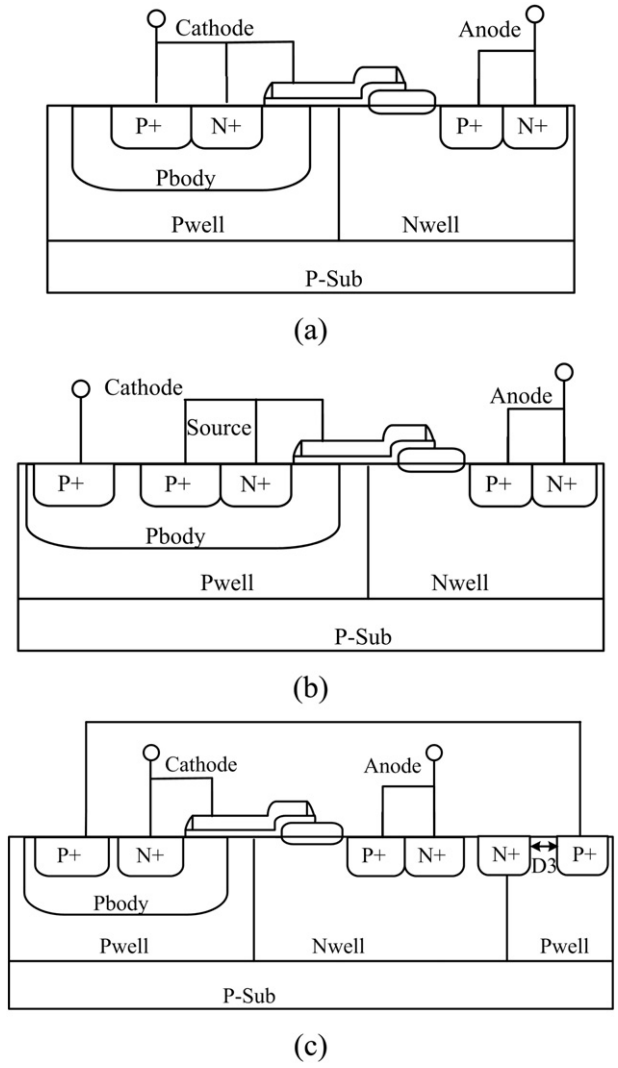

Fig. 1. Cross sections of LDMOS-SCR (a), HRLDMOS-SCR (b) and ZTLDMOS-SCR (c).

and HRLDMOS-SCR, the ZTLDMOS-SCR has a floating Zener-diode formed by the highly implanted n+ and p+ regions with a suitable spacing D_3 (shown in Fig. 2(c)), helping to decrease V_{t1}. The mechanism of these devices is confirmed by the TCAD simulations. Their internal electric field distributions before trigger are shown in Fig. 3. When these devices are stressed with the same ESD pulse, the barrier width of ZTLDMOS-SCR is much smaller, resulting in a lower V_{t1} than the other two devices. On the other hand, the current density of ZTLDMOS-SCR is the largest, resulting in the strongest ESD robustness.

The corresponding stripe layouts of the LDMOS-SCR, HRLDMOS-SCR and ZTLDMOS-SCR are shown in Fig. 2(a), (b) and (c). Firstly, by removing the stripe resistance of length D_1 shown in Fig. 2(b) from the source region, a discrete stripe resistance is obtained and connected with the cathode of LDMOS-SCR, the modified layout is shown in Fig. 2(d). Secondly, dividing the stripe resistance into three parts (A, B, and C), where the parts A and C having the same length D_2 and contact-hole are connected by the aluminum covering on part B without the contact-hole, helps to adjust the turn-on resistance and V_h of the HRLDMOS-SCR device. Finally, a square resistance is connected in series with the source of ZTLDMOS-SCR having the ring layout, as shown in Fig. 2(e), which improves the ESD performance including increasing the *FOM* for the optimized ZTLDMOS-SCR device.

3. Results and discussion

Experimental LDMOS-SCR, HRLDMOS-SCR and ZTLDMOS-SCR devices are fabricated in 0.25-μm, 0.35-μm and 0.5-μm BCD processes. Their ESD characteristics are tested using the Barth 4002 transmission line pulse (TLP) system with a pulse width of 100 ns and a rise time of 10 ns. The I_{t2} is obtained when the leakage current changes abruptly by more than 3 orders of magnitude under a fixed DC bias condition after each TLP test and the device enters into the second-breakdown state.

3.1. Optimizing the V_h of LDMOS-SCR devices

The TLP *I–V* curves of the LDMOS-SCR, HRLDMOS-SCR and ZTLDMOS-SCR devices fabricated in the 0.35-μm BCD process with the same *W* of 100 μm are shown in Fig. 4. The length D_1 (shown in Fig. 2(b)) of HRLDMOS-SCR is 3 μm. When the TLP pulse stressed on the LDMOS-SCR devices increases up to 72 V, the LDMOS-SCR devices are triggered and turned on, their V_{t1} values are all approximately 50 V. When the TLP pulse increases continually from 72 to 103 V and the DC bias keeps the same value, these devices are held on with a small leakage current, and their V_h values vary from 5 to 10 V. When the TLP pulse is further increased, the devices fail and the leakage current increases remarkably, and the I_{t2} varies from 5.5 to 3.3 A. The detailed ESD characteristics of the LDMOS-SCR, HRLDMOS-SCR and ZTLDMOS-SCR devices are shown in Table 1.

Compared to the LDMOS-SCR and HRLDMOS-SCR, the ZTLDMOS-SCR has the highest *FOM* and the lowest V_{t1}, but its smallest V_h is insufficient to resist the latch-up risk. Owing to the increased turn-on resistance, the HRLDMOS-SCR has the largest V_h. Moreover, the V_h can be further improved by increasing D_1 from 3 to 7 μm. The TLP *I–V* curves of HRLDMOS-SCR devices with different D_1 dimensions are shown in Fig. 5. When D_1 is increased from 3 to 5 μm, the V_{t1} and V_h increase slightly. When D_1 is further increased from 5 to 7 μm, I_{t2} decreases from 4.2 to 3.7 A, and V_h increases from 8.2 to 12.1 V. This behavior is due to the significantly increased current path.

In addition, V_h of the HRLDMOS-SCR device can be increased by decreasing D_2 (shown in Fig. 2(d)) while keeping the same *W* and D_1. The TLP *I–V* curves of HRLDMOS-SCR devices with different D_2 dimensions are shown in Fig. 6, and the ESD characteristics of HRLDMOS-SCR devices with different D_1 and D_2 are summarized in Table 2. When D_2 is decreased from 35 to 25 μm, the V_h increases continuously owing to the increased turn-on resistance, which is calculated approximately by the definition of $R = R_{\square} \times L/W_D$ [11], where $R_{\square}$ is a square resistance per unit area, *L* and W_D are the length and width of stripe resistance connected in series with the source of the LDMOS-SCR , respectively. Meanwhile, the *FOM* of the HRLDMOS-SCR increases from 0.29 to 0.58 mA/μm^2, when the D_2 is decreased to 25 μm.

3.2. Optimizing the V_{t1} and I_{t2} of LDMOS-SCR devices

The V_h and *FOM* of HRLDMOS-SCR can not be continually increased by decreasing the D_2, due to the restriction of ESD robustness. Compared to the LDMOS-SCR and HRLDMOS-SCR, the ZTLDMOS-SCR not only exhibits a significantly decreased V_{t1}, but also an increased I_{t2}, which is attributed to the Zener diode and the added current conduction path. Furthermore, V_{t1} can be decreased by shortening the spacing D_3 (shown in Fig. 2(c)). The TLP *I–V* curves of ZTLDMOS-SCR devices with different D_3 dimensions are shown in Fig. 7. When the D_3 decreases from 0.8 to 0.4 μm, the V_{t1} decreases from 17.1 to 7.0 V due to the punch-through of the reversed PN junction. When the D_3 continually decreases from 0.4 to 0 μm, the V_{t1} and I_{t2} change insignificantly, but the leakage current increases from the order of 10^{-10} to 10^{-3} A. Therefore, the ZTLDMOS-SCR device with too small D_3 is unsuitable for high voltage ESD protection due to the small V_{t1} and large leakage current.