Microelectronics Reliability 61 (2016) 120–124

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Investigation on LDMOS-SCR with high holding current for high voltage ESD protection

Hailian Liang, Xiuwen Bi, Xiaofeng Gu *, Huafeng Cao, Yun Zhang

Engineering Research Center of IoT Technology Applications (Ministry of Education), Department of Electronic Engineering, Jiangnan University, Wuxi 214122, China

ARTICLE INFO

Article history:
Received 15 September 2015
Received in revised form 5 January 2016
Accepted 26 January 2016
Available online 1 February 2016

Keywords:
Electrostatic discharge (ESD)
Latch-up
The lateral diffused metal-oxide semiconductor embedded in silicon controlled rectifier (LDMOS-SCR)
Holding current

ABSTRACT

We investigate a novel lateral diffused metal-oxide semiconductor (LDMOS) device embedded in silicon controlled rectifier (SCR) and resistance-capacitance circuit (LDMOS-SCR-RC). The internal RC-coupling effect helps to increase the holding current (I_h), resulting in the enhanced latch-up immunity of electrostatic discharge (ESD) protection device in high voltage integrated circuits (HV ICs). Transmission line pulse testing results show that the proposed LDMOS-SCR-RC has the largest I_h and smallest trigger voltage (V_{t1}), comparing to the conventional LDMOS-SCR and LDMOS-SCR embedded a resistance. When key parameters such as the gate-length and resistance are optimized, the I_h increases further from 1.1 A to 1.5 A, while the V_{t1} changes insignificantly. The detailed internal mechanism of LDMOS-SCR-RC with regard to key parameters is analyzed numerically by the SENTAURUS simulation. Results confirm that the increased I_h is mainly due to the enhanced RC-coupling effect. Finally, DC measurements conducted with a semiconductor curve tracer also confirm that the LDMOS-SCR-RC with small device area is effective for avoiding latch-up risks. The optimized LDMOS-SCR-RC provides a useful latch-up immune ESD protection solution for HV ICs input/output ports.

1. Introduction

The lateral diffused metal-oxide semiconductor embedded in silicon controlled rectifier (LDMOS-SCR) is widely used as output driver and electrostatic discharge (ESD) self-protection device in high voltage integrated circuits (HV ICs) due to its high breakdown voltage and low turn-on resistance [1–2]. However, with the feature size of HV ICs scaling down, LDMOS-SCR served as ESD protection is greatly limited by its weak latch-up immunity. When the operation voltage of HV ICs is between 20 V and 40 V, the ESD protection design based on LDMOS-SCR structure in HV ICs is becoming more difficult to improve the latch-up immunity. ESD protection devices for HV ICs require by a reasonable trigger voltage (V_{t1}), a high holding voltage (V_h) and strong ESD robustness within a small device area. Generally, the latch-up immunity is determined by the V_h and the holding current (I_h). Several methods have been developed to increase V_h, including reducing the electron emission rate [3], embedding the bipolar junction transistor (BJT) in a conventional SCR [4] and optimizing the source side engineering [5]. However, the consumed silicon area and the latch-up risk of LDMOS-SCR could not be sufficiently minimized by using these methods. Mergens et al. proposed a method to decrease the latch-up risk by increasing I_h [6], but it was only suitable for low voltage ESD protection and still consumed a large silicon area due to using the MOS with an external RC circuit.

In this paper, we investigate a novel structure of LDMOS-SCR containing an internal RC circuit (LDMOS-SCR-RC). The ESD characteristics of LDMOS-SCR-RC devices with different key parameters such as gate length and resistance are studied by SENTAURUS simulations. Results of DC and transmission line pulse (TLP) measurements confirm that the optimized LDMOS-SCR-RC has improved latch-up immunity, making it an attractive device for constructing effective ESD protection solutions for input/output (I/O) ports of HV ICs.

2. Device structures design and schematic analyses

The cross sections and equivalent circuits of conventional LDMOS-SCR [7], LDMOS-SCR with an embedded resistance (LDMOS-SCR-R), and LDMOS-SCR-RC are shown in Fig. 1. Unlike the conventional LDMOS-SCR, the latter two devices have RC-coupling effect, due to the parasitic resistance R_{p2}, gate drain capacitance C_{gd}, gate oxide capacitance C_{ox}, gate source capacitance C_{gs} and the parasitic capacitance C_D resulted by the reversed PN junction. The RC-coupling effect can help decreasing the V_{t1} and increasing the trigger current because of the floating gate and equivalent capacitance resulted from the C_{ox} and C_{gs} connecting in parallel.

Compared to the conventional LDMOS-SCR, the LDMOS-SCR-R has an embedded p-type well resistance, which is connected with the source and gate. Its purpose is to increase the turn-on resistance as well as V_h. When a small ESD voltage with a short rise time of 10 ns is applied to the LDMOS-SCR-R, the minority carrier drift current resulting from the reversed PN junction and the parasitic RC-coupling effect

* Corresponding author at: Department of Electronic Engineering, Jiangnan University, 1800 Lihu Avenue, Wuxi, Jiangsu, 214122, China.
E-mail address: xgu@jiangnan.edu.cn (X. Gu).

http://dx.doi.org/10.1016/j.microrel.2016.01.016
0026-2714/

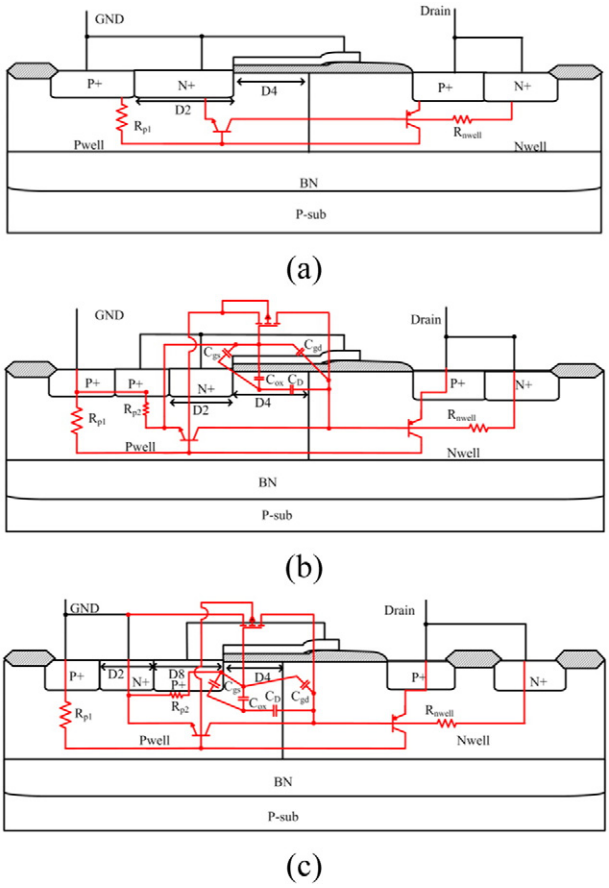

Fig. 1. Cross sections and internal equivalent circuits of LDMOS-SCR (a), LDMOS-SCR-R (b), and LDMOS-SCR-RC (c).

increases quickly, leading to the turning on of parasitic SCR in the LDMOS-SCR-R. However, the resistance R_{p2} in series with the SCR weakens the ESD robustness when the turn-on resistance and V_h of LDMOS-SCR-R increase.

We sandwich the novel source between the highly implanted p + region in series with the ground and the p-type well resistance in series with the gate, and connect the source with the ground. As a result, both V_h and I_h of the LDMOS-SCR-RC increase due to the decreased electron emissivity and increased trigger current, respectively. Compared to the LDMOS-SCR-R, the equivalent circuit of LDMOS-SCR-RC has a smaller turn-on resistance, since the resistance R_{p2} disappears in the SCR ESD current path. Furthermore, the p + region connected with the gate increases the R_{p2}, resulting in the larger trigger current and I_h. In addition, effects of the gate length D_4, the stripe resistance length D_8, and the source regions length D_2, as shown in Fig. 1(c), on improving the ESD performance of LDMOS-SCR-RC are investigated experimentally and by simulations.

Optical micrographs of the LDMOS-SCR-RC and the LDMOS-SCR triggered by an external RC circuit are shown in Fig. 2 (a) and (b), respectively. The device area of LDMOS-SCR-RC is 900 μm^2, while the LDMOS-SCR triggered by an external RC circuit has an extra silicon area of 850 μm^2 due to the discrete resistance and MOS transistor functioning as a capacitance. Both devices have a decreased V_{t1} since a weakened conduction channel forms by the RC-coupling effect, but the trigger current and I_h of the LDMOS-SCR triggered by an external RC circuit are independent of the external RC-coupling effect. In other words, the internal RC-coupling effect, resulting from the embedded RC circuit in the LDMOS-SCR-RC, makes more significant contributions to increase I_h than the external RC-coupling effect.

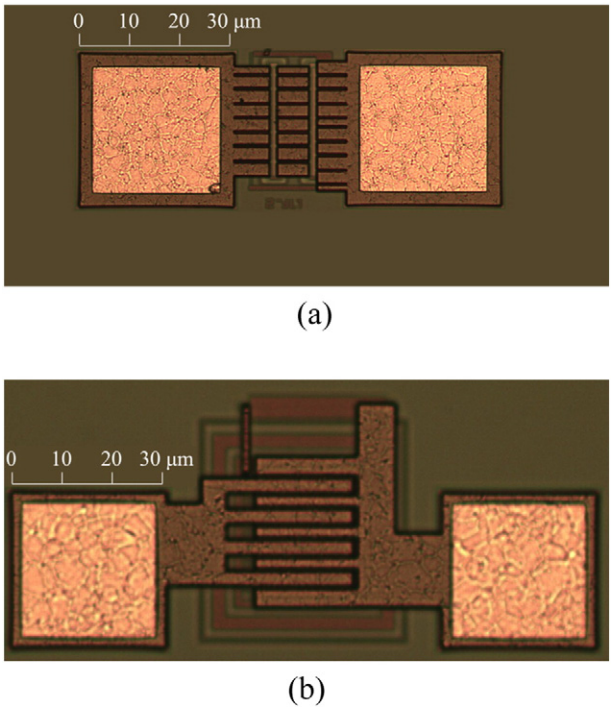

Fig. 2. Micrographs of LDMOS-SCR-RC (a) and LDMOS-SCR with an external RC circuit (b).

3. Results and discussion

Experimental devices are fabricated in a 0.25-μm 18-V Bipolar CMOS DMOS (BCD) process. Their ESD characteristics are measured by using a Barth 4002 TLP system with a pulse width of 100 ns and a rising time of 10 ns [8]. The failure current (I_{t2}) is recorded when the leakage current changes abruptly by more than three orders of magnitude under a 20-V bias after each TLP test, and the tested device enters the second-breakdown state. According to the Barth 4002 TLP system, $I_{t2} \times 1500$ V is defined as the highest tolerance voltage of ESD protection devices under the human body model (HBM). The transient response of the LDMOS-SCR-RC is investigated by TCAD simulations with a series of ESD current pulse of 10 ns rising time and 100 ns period time. The DC characteristics of LDMOS-SCR-R are measured with the TEKTRONIX 370B curve tracer.

3.1. ESD characteristics of experimental devices

The TLP *I-V* curves LDMOS-SCR, LDMOS-SCR-R and LDMOS-SCR-RC having a total area (S) of about 900 μm^2 are shown in Fig. 3. With the exception of LDMOS-SCR-RC, the other two devices display a rapid snapback after triggering. The LDMOS-SCR-R has the largest V_h and smallest I_{t2}, due to the R_{p2} in series with the turned-on SCR. However, the largest V_h (6.9 V) is still insufficient to reduce the latch-up risk with respect to the operation voltage (18 V) of protected circuits. The LDMOS-SCR-RC has the largest I_h (1.1 A), which is sufficiently high to reduce the latch-up risk, regarding to the electrical characteristics of I/O ports of protected HV ICs.

Meanwhile, the effect of RC-coupling on the I_h of ESD protection devices is investigated by comparing the LDMOS-SCR-RC and LDMOS-SCR triggered by an external RC circuit. Compared to the LDMOS-SCR triggered by an external RC circuit, the LDMOS-SCR-RC has smaller V_{t1}, larger I_{t2} and I_h, which consistent with our analyses of internal and external RC-coupling effect of LDMOS-SCR-based devices. In addition, the figure of merit (*FOM*, defined by I_{t2}/S) [9] of the LDMOS-SCR-RC increases about two times. The detailed parameters of experimental devices are listed in Table 1, and ESD performance parameters provided by the ESD design window of HV ICs are listed in Table 2. In general, V_{t1} should