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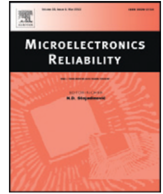

300-V class power n-channel LDMOS transistor implemented in 0.18-μm silicon-on-insulator (SOI) technology

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ABSTRACT

A SOI platform is developed for a LDMOS transistor from 70 V to 300 V. It is one of the best cases covering the wide voltage range. By applying novel DTI technology, the pitch of a single LDMOS transistor cell is reduced. Thin silicon and oxide film help to reduce the process complexity and the cost of SOI wafer. The platform is compatible with standard CMOS technology, and is appreciable for broad power IC products.

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1. Introduction

In the area of modern power device design, silicon-on-insulator (SOI) technology has been widely investigated for the purpose of its ideal substrate isolation, strong immunity to latch-up effect, small isolation area and low leakage current. These pretty good performances make the SOI technology the best choice for HV and power applications like automotive, industry, medical and space field. Many technologies have been proposed for SOI power device design, such as partial depleted SOI lateral diffusion metal-oxide-silicon field effect transistor (PDSOI-LDMOS) [1], lateral insulated gate bipolar transistor (LIGBT) [2], 3D-RESURF device [3], and super junction LDMOS [4]. However, most of these devices involve fabrication complexity and are difficult for power integration circuit (PIC) production. PDSOI-LDMOS needs extra processes to open the oxide window beneath the drain terminal. Fully depleted LDMOS on SOI is still the most convenient technology to be manufactured and integrated [5,6].

2. Process compatibility and improvement

In this paper, a 0.18 μm SOI Bipolar–CMOS–DMOS (BCD) process platform covering a voltage range from 70 to 300 V is presented. The detailed process information is shown in Table 1. Breakdown voltage for a 300 V n-channel LDMOS is 352 V with a specific ON-Resistance of 1860 mΩ-mm^2. Thickness of both SOI layer and buried oxide (BOX) is about 2 μm in our development. The thin SOI layer used in our platform can reduce the difficulty and cost of deep trench etching and filling. Besides, better thermal dissipation ability is also achieved by using thin BOX.

The brief process flow is described in Fig. 1. The resistivity of the SOI wafer is fully compatible with the standard CMOS process. Compared to the standard 1.8 V/5 V CMOS process, two additional steps, DTI (Deep Trench Isolation) definition and drift region implantation, are added for high voltage power devices.

Deep trench isolation plays an important role in SOI technology. Oxide–poly–oxide structure trench has been widely used in power technology for isolation due to its great stress balance performance [7]. However, the poly inside the oxide will enlarge the lateral size for higher isolation voltage applications, since the poly shares no voltage drop when high voltage is dropped across the trench structure. Take 2-μm width trench for example, TCAD simulation structures and electric potential contours of oxide–poly–oxide trench and oxide-only trench are shown in Fig. 2(a) and (b), respectively. For conventional isolation trench (i.e. oxide–poly–oxide structure), voltage drops only across the oxide layer around the poly plug, while voltage drops uniformly across the whole trench width for the oxide-only trench structure. The TCAD simulated electric potential value along the cutline is also shown in Fig. 3(a), and there is a flat electric potential area in the conventional structure since there is no voltage drop across the poly. As for the electric field along the cutline, shown in Fig. 3(b), the oxide-only trench structure presents lower peak value of electric field (~2 MV/cm) compared with conventional trench (~3.5 MV/cm) for same trench width. As a result, the proposed oxide-only trench structure has a better

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Table 1
Detailed process information list of our SOI technology.

Device	Parameter
Process	0.18-μm SOI
Isolation	DTI: Deep trench isolation
Photo layers	16L (4M to 6M for option)
LV-CMOS	N/P: 1.8 V/5 V
HV-LDMOS	N/P: 70 V, 120 V, 200 V, 300 V (P for option)
Diode	Zener, LV, HV: 70 V–300 V
Zener	BV = 5.7 V, Tc < 200 ppm/°C
BJT	High-performance-NPN, LNPN, LPNP
Resistor	Poly-Si, Diff.
Capacitor	1 fF/μm^2, 2 fF/μm^2
HRI	Rs = 1 kΩ/sq
MRI	Rs = 400 Ω/sq

electric field endurable ability, which is important for isolation. To achieve the same level of breakdown voltage, the isolation area can be reduced by at least 50% applying oxide-only trench compared with the oxide–poly–oxide structure. However, a big challenge for oxide-only trench is the stress problem due to the different inflation coefficients at the interface between the oxide and the silicon, which will bring severe wafer warping issue. Warping issue could further induce the thickness uniformity problem of deposition films. Fig. 4 shows the thickness uniformity comparison of one deposition film before and after process optimization. It is clearly found that the uniformity problem has been solved by the optimized process.

3. Device design and fabrication

In our platform, LDMOS works under fully depleted mode. The critical electric filed $E_{C\text{-}Si}$ in silicon follows [8,9]:

$$E_{C-Si} = \left(\frac{q(n+1)N_D}{B\varepsilon_{Si}}\right)^{\frac{1}{n+1}}, \tag{1}$$

$$B = \frac{1.06\times10^6/\text{cm}}{E_0^n \exp(n)}, \tag{2}$$

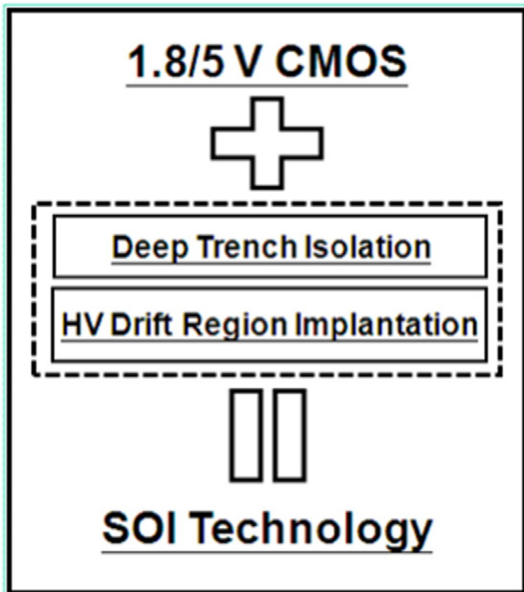


Fig. 1. Process flow compatible with 1.8/5 V standard CMOS.

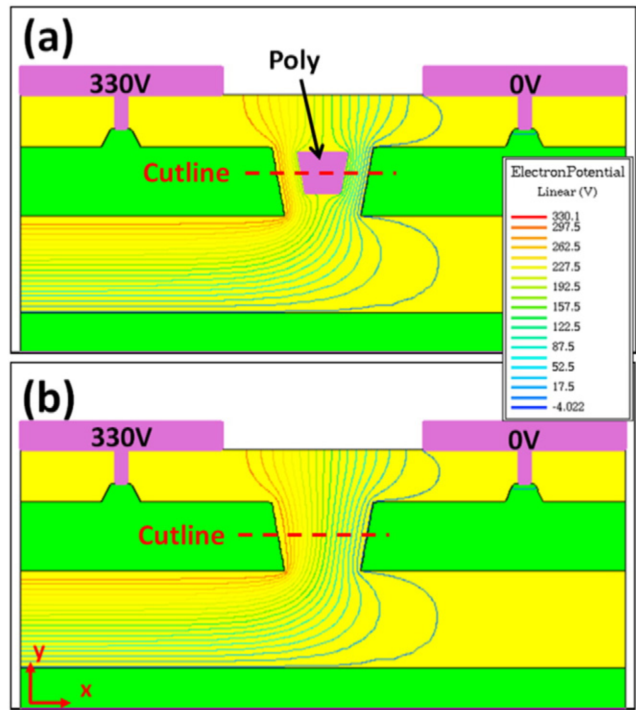
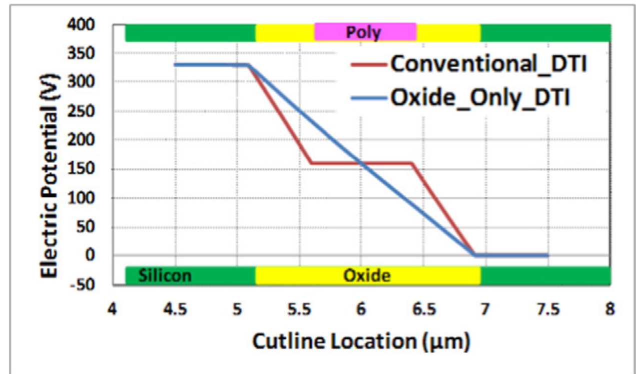
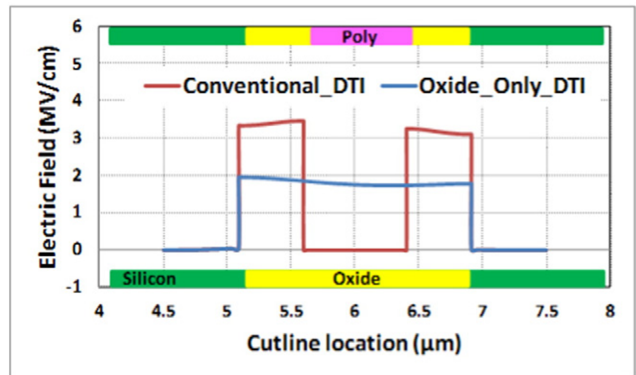


Fig. 2. Structure and electric potential contours of conventional oxide–poly–oxide trench (a) and oxide-only trench (b).



(a)



(b)

Fig. 3. Value of electric potential (a) and electric field (b) for conventional and oxide-only trench structure.

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