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Simulating the effect of lifetime non-uniformity on solar cell performance using cmd-PC1D 6 and Griddler 2

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Abstract

In this paper we present a novel approach to investigate the influence of non-uniformity in the minority carrier lifetime of c-Si wafers on solar cell efficiency. By using a combination of one-dimensional device modelling (cmd-PC1D 6) and finite element circuit modelling (Griddler 2) we are able to simulate the total IV characteristics of a solar cell based on input from minority carrier lifetime images. With suitable input regarding the optical properties, doping profiles, recombination behaviour and sheet resistance of the passivated and metallized surfaces involved this combined model can be used to predict the total cell efficiency of mc-Si solar cells and other cells with significant lateral variations in wafer quality. Several artificial test cases are investigated in order to determine the sensitivity of the method and the magnitude of the effect of lifetime distribution. We find that using the weighted average of the two-diode parameters J_{01}, J_{02} and J_{light} in most cases provides a good description of total cell performance, correctly describing the IV parameters within an error of ~0.1 - 0.2 % relative as compared to simulations taking the complete lateral distribution over the wafer into account. The deviation was however observed to be up to 1.5% for extreme, artificial cases. By instead assuming an average carrier lifetime over the wafer larger errors are observed, due to the non-linear relation between the two-diode parameters and the bulk lifetime.

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1. Introduction

Directionally solidified multicrystalline silicon (mc-Si) is widely used in the photovoltaic industry due to the cost effective production process. The performance of mc-Si solar cells is, however, limited by recombination active impurities and extended crystal defects. Throughout the solidification process the crystal quality of conventional mc-Si deteriorates due to incorporation of impurities and generation and multiplication of crystal defects, such as grain boundaries and dislocations. Negative effects of impurities on the cell efficiency can to a certain degree be mitigated, e.g. by phosphorus gettering of metallic impurities during the emitter in-diffusion [1]. Thus, grain boundaries and especially dislocations are considered more detrimental to the cell performance in mc-Si solar cells. These dislocations, typically originating in grain boundaries, grow with the height in the ingot becoming increasingly dominating towards the top of conventional mc-Si [2]. Such localized areas of high dislocation density and corresponding low carrier lifetime reduce the solar cell performance considerably in wafers from the top part of ingots [3]. Recent improvements in directional solidification has reduced the dislocation growth considerably [4]. Seed assisted growth is used in production of high performance multicrystalline silicon (HPMC-Si), where it is believed the initial grain boundary orientation as well as the smaller grain size abates the growth of dislocation clusters. Still, the minority carrier lifetime of mc-Si still may vary considerably over the wafer. Using imaging techniques such as band-to-band photoluminescence imaging lifetimes can be determined with high spatial resolution [5], [6]. It is common to include the bulk carrier lifetime into simulations models to account for the influence of wafer quality on cell performance. However, it is generally not possible to include the effect of the *distribution* of the lifetime over the wafer into standard semiconductor simulation tools due to prohibitively large size of the simulation area. The importance of the lateral distribution of the carrier lifetime is therefore an important question which is not straightforward to answer. In this paper we attempt to quantify the impact of lifetime variations with a combined approach using both local one-dimensional device simulations and a full-cell equivalent circuit model.

2. Simulation approach

This work attempts to combine the powers of two different simulations tools: cmd-PC1D 6.2 (and the user interface version PC1Dmod 6.1) are modification of the popular semiconductor device simulator PC1D [7], [8] with an updated physics engine, improved models for c-Si and the added option of running simulations from the command line. The program provides an easy and efficient way for solving the coupled nonlinear equations for carrier generation, recombination and transport in the device, but is limited to one dimensional structures [9], [10]. On the other hand, Griddler 2.5 is a finite element method solver for simulating a vast network of lumped circuit elements, designed to analyze the full metallization pattern in a complete solar cell [11], [12]. The program also allows for importing or drawing images of diode parameters, sheet resistances, light intensity, etc., thus enabling investigations of lateral variations in these quantities. In this paper we show how cmd-PC1D 6.2 together with a suitable cell model can be used to generate maps of the two-diode parameters J_{01}, J_{02} and J_{ligth} for both passivated and metallized areas, which can then be used as input for Griddler 2. A schematic illustration of the total simulation process from lifetime map to IV curve is shown in Fig. 1. Note that the added flexibility obtained by running cmd-PC1D 6 simulations from the command line enables us to fully automate this process, and it is therefore possible to e.g. run through a large series of lifetime images or provide feedback from the simulation results back to the cell parameters in the cmd-PC1D 6 model.

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