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ScienceDirect

Energy Procedia 92 (2016) 412 – 418

Energy Procedia

6th International Conference on Silicon Photovoltaics, SiliconPV 2016

Recombination behavior of photolithography-free back junction back contact solar cells with carrier-selective polysilicon on oxide junctions for both polarities

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Abstract

We report on ion-implanted, inkjet patterned back junction back contact silicon solar cells with **POL**ysilicon on **O**xide (POLO) junctions for both polarities – n^+ doped BSF and p^+ doped emitter. The recombination behavior is investigated at two different processing stages: before and after trench separation of p^+ and n^+ regions within polysilicon (poly-Si). Before trench separation, we find a systematic dependence of the recombination behavior on the BSF index, i.e. the p^+n^+-junction meander length in the poly-Si. Obviously, recombination at the p^+n^+-junction in the poly-Si limits the implied open circuit voltage $V_{oc,impl.}$ at one sun illumination and the implied pseudo fill factor $pFF_{impl.}$ to 695 mV and 80 %, respectively. After trench isolation, however, $V_{oc,impl}$ ($pFF_{impl.}$) values increase up to 730 mV (85.5 %), corresponding to a pseudo-efficiency of 26.2 % for an assumed short circuit current density J_{sc} of 42 mA/cm^2. We demonstrate a photolithography-free back junction back contacted solar cell with p-type and n-type POLO junctions with an in-house measured champion efficiency of 23.9 % on a designated area of 3.97 cm^2. This efficiency is mainly limited by the imperfect passivation in the undoped trench regions and at the undoped front side.

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Peer review by the scientific conference committee of SiliconPV 2016 under responsibility of PSE AG.

Keywords: back junction back contact solar cell; polysilicon on oxide junctions; POLO; *pn* junction; trench isolation; recombination

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Peer review by the scientific conference committee of SiliconPV 2016 under responsibility of PSE AG.
doi:10.1016/j.egypro.2016.07.121

1. Introduction

In recent years many research groups have investigated different types of carrier-selective junctions for high efficiency silicon solar cells [1]. The back junction back contact (BJBC) cell with hydrogenated amorphous silicon (*a*-Si:H)/ monocrystalline silicon (*c*-Si) heterojunctions, reaching an energy conversion efficiency of 25.6 % [2], is an excellent and well-known example for carrier-selective junctions, which were integrated into high efficiency silicon solar cells. A drawback of the *a*-Si/*c*-Si heterojunction technology for the application in BJBC cells is the restriction to low temperature processing and therefore a rather complex pattering procedure for the formation of interdigitated junctions and metallization on the rear side [3]. Shadow masked ion implantation is an enabling local doping technique for the junction formation on the rear side of BJBC cells to reduce the process complexity [4-8]. Nevertheless thermal stability of the junctions is required therefor.

In the late 1970s and early 1980s different groups proposed polysilicon emitters with an interfacial oxide as carrier-selective junctions for silicon solar cells with high temperature stability [9-13]. This type of junctions are denoted as **POL**ysilicon on **O**xide (POLO) junctions in the following [14-16]. Excellent results have recently been achieved with these junctions. In particular, saturation current densities as low as for *a*-Si/*c*-Si junctions, but lower junction resistivities for both electron collecting junctions based on n^+ POLO and hole collecting junctions based on p^+ POLO have been achieved [1,15,17-22]. This comparison between *a*-Si/*c*-Si heterojunctions and our temperature stable POLO junctions implies an efficiency potential larger than 25 % for both approaches and a potentially reduced process complexity for the latter [8].

So far, many groups [17-21] have reported promising implied open circuit voltages and pseudo fill factors for test structures and BJBC cell precursors with POLO junctions for both polarities. Yang *et al.* just recently published first photolithography patterned POLO-BJBC solar cells with an efficiency of 19.2 % [21].

One key challenge for the integration of these junctions into BJBC cells is the poor recombination behavior of *pn*-junctions formed within highly defective poly-Si [23, 20]. We therefore investigate the influence of a trench, separating p^+ and n^+ regions within poly-Si, on the recombination behavior on cells. We show promising results for BJBC solar cells with POLO junctions for both polarities with an in-house measured efficiency of 23.9 % (designated area of 3.97 cm^2). As patterning technique, we use inkjet-printed masks (which eventually can be substituted by screen printed masks) in combination with wet chemical etching. Although local doping is envisaged to be eventually performed via masked ion implantation, we also use inkjet printing for patterning of dielectric implant masks here to mimic masked ion implantation, but with a more flexible mask for the evaluation of different cell geometries.

2. Experimental

We use saw-damage etched 156 mm × 156 mm *n*-type Czochralski silicon wafers with a base resistivity of 3.5 Ωcm and a thickness of 160 µm as substrate material. In order to blind out resistive losses in the metallization as well as busbar losses in a first step, 20 small cells with an active cell area of 20 mm × 20 mm are processed on each wafer. In addition, full-area implanted boron and counterdoped (boron overcompensated by phosphorus) reference regions are integrated on the wafer to facilitate process monitoring.

After growing a ~2.1 nm thin thermal silicon dioxide layer in a tube furnace, undoped amorphous silicon (*a*-Si) is deposited on both sides by using low pressure chemical vapor deposition (LPCVD). Hereafter the front (rear) side of the wafer receives a blanket phosphorus (boron) implantation, followed by a masked phosphorus implantation on the rear.

The latter locally overcompensates the boron in an interdigitated pattern with different BSF indices ranging from 730 µm to 1175 µm (Fig. 1a). For masking of the phosphorus implantation, we pattern a sputtered dielectric layer by inkjet-printed hotmelt wax and a subsequent wet-chemical etching.

After removal of the dielectric implant mask, high temperature treatment for the formation of the POLO junctions (dopant activation, crystallization of the *a*-Si, and perhaps local break-up of the interfacial oxide) is performed. During this step, a thick silicon dioxide layer is grown on top of the poly-Si by wet thermal oxidation. Subsequently, this silicon dioxide layer is again patterned via inkjet printing on the rear, and removed from the front side of the wafer. The remaining SiO_2 on the rear acts as etching barrier for a subsequent texturization process, which yields a

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