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Investigations on the formation of stacking fault-like PID-shunts

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Abstract

Potential-induced degradation of the shunting type (PID-s) of silicon solar cells is attributed to planar defects at the cell front surface. Stacking fault crystal defects with a length of few micrometers penetrating the p-n junction cause shunts when they are decorated with Na atoms. The target of this work is to improve knowledge on the formation of these stacking fault defects.
Two approaches are utilized to find out if stacking faults develop during the cell process or if they evolve from defect nuclei during PID-stress. One approach is chemical defect etching and subsequent microscopy of stacking fault related signatures. Statistical evaluation of etched defects on cell areas with and without PID-s indicates that stacking faults are not present before PID stress is applied to the solar cell. The second approach utilizes iterative SEM/EBIC imaging of PID-shunts in the course of proceeding degradation. EBIC investigations after each PID test reveal that a fraction of investigated stacking faults grow as a function of the PID stress duration.
It is concluded that stacking faults grow under the influence of Na penetration. It is assumed that nuclei for the formation of stacking faults are microscopic defects such as dislocations or precipitates associated with surface defects on the silicon surface.

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Keywords: Potential-induced degradation; silicon; solar cell; stacking fault; shunting; defects

1. Introduction

Potential-induced degradation (PID) of PV modules containing crystalline silicon solar cells is a topic of sustained scientific interest [1-3]. PID of the shunting type (PID-s) has the most detrimental impact on the reliability

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and yield of installed modules. PID-shunts are attributed to Na decorated, planar crystal defects (stacking faults) penetrating the p-n junction of solar cells [4]. Up to now it is not clear how (and when) the stacking faults emerge. In particular, it is not clear if they already form during the cell process or if they evolve during the PID-stress. This is of high interest since an increased knowledge about the generation mechanism of stacking faults would enable more direct measures for PID-s stability on the very cell level. The aim of this work is to find out whether stacking faults already exist before their electrical activation by PID stress. Planar and polished model solar cells are used in order to monitor the evolution of particular stacking faults in great detail. Two approaches are pursued: (1) evaluation of stacking fault densities of linear etch marks after delineation of crystal defects, and (2) iterative PID testing and monitoring of shape and size of individual electrically active stacking faults.

2. Experimental

A monocrystalline solar cell (p-type base) with polished front side, diffused P front side emitter and SiN antireflective coating has been exposed to PID stress using the PID cell test setup 'PIDcon' by Freiberg Instruments. The top electrode has been put on a layer stack consisting of EVA encapsulant polymer and soda-lime glass mimicking the front side of a solar module [5]. The degradation has been performed over a time period of 24 hours at a temperature of 85 °C and with +1000 volts at the top electrode with respect to the grounded solar cell. Shunted cell areas have been localized with photoluminescence (PL). Two samples with a size of 0.8x0.8 cm² have been prepared out of the cell area affected by PID-s and of unaffected regions, respectively. Microscopic verification of PID-shunts has been done by scanning electron microscopy (SEM) using the electron beam induced current (EBIC) method in the Hitachi SU-70 SEM equipped with the DISS5 lock-in EBIC system by point electronic. Then, a two-step wet chemical etch process has been done to remove the silicon nitride layer and subsequently delineate the PID-shunts by defect etching [6]. Etch marks are identified by SEM and optical microscopy. The statistical evaluation is conducted both by a semi-automated image processing algorithm based on the software ImageJ 1.38 and by manual counting of delineated stacking faults in optical micrographs.

The stepwise degradation is performed at a 1x1 cm² sized piece of a similar solar cell with polished front side. It is gradually degraded on an area of 0.5 cm² using a customized PID cell test setup at 85 °C and a high voltage of +600 V. The high voltage is applied to the glass surface of the glass/EVA stack which is placed on the cell piece. The shunt resistance of the cell sample is monitored by means of in-situ current measurement at a reverse bias of 0.5 V. After each PID test the EVA foil and glass are carefully removed for SEM/EBIC imaging. PID cell tests and EBIC imaging of resulting PID-shunts are applied in an iterative sequence.

3. Results

3.1. Correlation of surface defects with PID-shunts after delineation by etching

A sample with PID-shunting is separated from the solar cell area that was subject to the PID cell test as described above. Before defect etching the sample is investigated by SEM/EBIC. EBIC investigations reveal PID-shunts by their typical signature (blurred spots with decreased EBIC signal, see inset in Fig. 1). Furthermore, at a reduced acceleration voltage of 5 kV the PID-shunts are characterized by dark lines and a weak EBIC contrast at one side of each line.

After defect etching, PID-shunt positions are imaged by optical microscopy. The optical microscopy image in Fig. 1 shows five etch grooves exactly at the positions where PID-shunts were visible in EBIC (inset) before etching. The etch grooves are parallel to the <011> crystal directions (0° or 90° in this image).