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PID- and UVID-free n-type solar cells and modules

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Abstract

In this paper we report on the high stability of our n-type front junction solar cells (n-PERT) exposed to potential-induced degradation (PID) and UV-induced degradation (UVID) conditions. These intrinsically stable n-Pasha cells enable PID- and UVID-resistant modules even with industrially low-cost standard EVA encapsulant, independent of system grounding and system voltage. Based on intentional modifications of the Boron emitter and/or the dielectric layer in the PID-free and UVID-free n-Pasha solar cells, we are able to replicate reported degradation effects and study the mechanisms behind it. A combination of altering the boron profile and the dielectric properties together with increasing the interface defect density D_{it} is detrimental for the stability. Applying our standard optimal B-diffusion and passivation scheme assure that the UV radiation and system voltage have virtually no effect on our n-Pasha cell and module performance.

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Keywords: PID, Potential Induced Degradation, UVID, UV Induced Degradation, n-Pasha, n-PERT, stability, degradation, dielectric, emitter

1. Introduction

In this paper we present potential-induced degradation (PID) and UV-induced degradation (UVID) resistant n-type c-Si solar cells enabling PID- and UVID-resistant modules even with common ethyl vinyl acetate (EVA) encapsulant, and independent of system grounding and system voltage.

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The PID effect is a power loss of photovoltaic modules due to applied high system voltage. It has mainly been observed in standard front junction p-type c-Si modules [1]. The degradation mechanism has been attributed to massive shunting (*FF* loss) caused by Na^+ ions bridging across the emitter [2]. PID was also observed in rear-contact IBC n-type cells and related to polarization effects leading to a passivation loss [3]. Although our n-Pasha (Passivated all sides H-pattern) cells and modules are resistant to PID and UV exposure, it has recently been reported that front junction (FJ) n-type based modules can suffer from PID [4, 5]. In contrast to p-type, no *FF* reduction but I_{sc} and V_{oc} loss was observed. The degradation was attributed to increased surface recombination [4] though the exact mechanism was still unclear. Similarly, a passivation loss was observed while exposing n-PERT (Passivated Emitter, Rear Totally Diffused) cells [6] to UV radiation resulting in UV-induced degradation (UVID).

As PID occurs at negative voltages for p-type cells [2] and at positive voltages for n-type IBC (Interdigitated Back Contact) cells [3] or n-PERT cells [5,7], PID can be prevented by grounding the system, respectively, at the negative and the positive connector/pole, thus preventing the degradation inducing system voltages. However, this solution is not possible with 'floating' PV systems and halves the possible voltage range for grounded systems, thus increasing the balance of system costs.

The amount of PID in PV modules can be strongly reduced by applying encapsulants with higher electrical resistance thus reducing the polarization effects [5,7]. However, the cost of these encapsulants, like e.g. polyolefin, is higher than for commonly used EVA.

During the development of our n-Pasha cells over the past years, a thorough understanding has been built up on why our n-type c-Si solar cells are both PID- and UVID-free. We present results on cells with intentionally modified dielectrics and emitters to demonstrate the effect dielectrics and emitter profiles can have on PID and UVID. We also present modelling studies showing the degradation effects are consistent with deteriorating surface passivation. Our PID- and UVID-free cells presented in this paper can be integrated in modules without the necessity of using non-standard (and more expensive) encapsulants, and without restrictions on the system voltage range and on the choice or absence of grounding, providing a low-cost solution to manufacture UVID- and PID-resistant modules.

2. Approach

2.1. Cell preparation

The n-Pasha cells (Cz Si, 156x156 mm^2 semi-square) are prepared according to standard industrial processes on industrial tools. The cross-section of such n-Pasha cell is presented in Fig. 1. Intentionally introduced modifications into the processing of the Boron (B)-emitter and the dielectric front side layer were applied to reproduce degradation effects that have been observed by others [4,5]. Table 1 summarizes the modifications for the different samples. These variations did not significantly affect initial cell efficiencies. For PID testing, cells with soldered tabs are laminated into (single-cell) mini-modules using a commercial, fast-cure EVA encapsulant. A selection of non-laminated n-Pasha cells, produced together with the cells for PID tests, undergoes UVID testing.

Table 1. Overview of the intentional modifications and performed tests for the standard and experimental groups.

	Standard	Experimental 1	Experimental 2	Experimental 3	Experimental 4
Boron emitter	stable	modified	modified	Stable	modified
Dielectric	stable	stable	modified A	modified B	modified B
PID test	yes	yes	yes	yes	yes
UVID test	yes	yes	no	no	yes