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Minority carrier lifetime of n-type mono-crystalline silicon produced by continuous Czochralski technology and its effect on hetero-junction solar cells

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Abstract

The efficient use of the ingot material and high productivity of the continuous Czochralski (CCz) technology can help reduce the cost of n-type wafers which is one of the obstacles to the adoption of high performance n-type solar cells. Previous work has shown that 800 kg of n-type mono-crystalline ingot produced by CCz technology from a single crucible can be used to fabricate nPERT and n-Pasha solar cells with uniform performance despite the change of the minority carrier lifetime (MCLT) from the first to the last ingot. In this work, additional ingot characterizations have been done and higher performing hetero-junction (HJT) cells which are more sensitive to MCLT have been fabricated and characterized using the CCz wafers. Equivalent cell performance from CCz ingot to ingot pulled from a single run and between CCz and Cz has been demonstrated.

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Keywords: Minority carrier lifetime; Continuous Czochralski; CCz; Heterojunction; HJT; Mono-crystalline; n-type; n-Pasha

1. Introduction

Continuous Czochralski (CCz) technology has a greater potential for reducing production cost of the n-type mono-crystalline wafers over conventional Czochralski (Cz) because of two technological advantages: (1). CCz can maximize the usable material by pulling the ingots with tight distribution of resistivity (R_s) and interstitial oxygen

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concentration (O_i) throughout the ingot and (2). CCz can increase the production throughput and lower the consumable cost by pulling 800 kg of ingots in a single run from the same crucible. However, due to the gradual accumulation of the impurities in the silicon melt as more ingot material is pulled from the crucible, the minority carrier lifetime (MCLT) of the ingots pulled from the same run can change from several thousand microseconds for the first ingot to 1000 microseconds for the last ingot. Study has been done previously to determine the effect of this impurity accumulation on the performance of nPERT and n-Pasha solar cells [1]. In Figure 1, the published data from the previous study and the data from additional cell processing run after the publication have been combined to show that the solar cells fabricated on wafers cut from different segments of the entire 800 kg of ingots with different MCLT is virtually the same indicating material with MCLT >1000μs is adequate to achieve good cell performance. On the other hand, since the nPERT and n-Pasha are not the highest performing n-type solar cell technology with the cell efficiency just above 20%, the work has been extended to higher performing hetero-junction (HJT) cells which utilizes amorphous silicon thin layers to achieve excellent surface passivation [2]. As the result of this improved surface passivation, HJT cell efficiency is very dependent on incoming wafer quality [2, 3]. The MCLT, R_s and O_i will all impact the performance of the HJT cells. This paper focuses on the MCLT characterization of n-type mono-crystalline silicon produced by CCz technology and its effect on HJT solar cell performance.

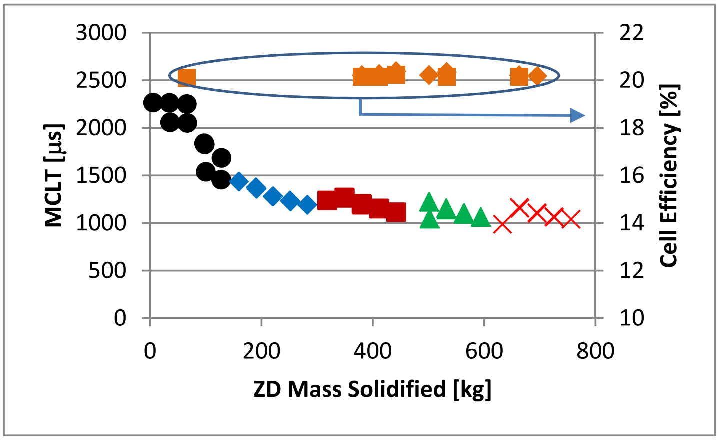

Fig. 1. MCLT and n-Pasha cell efficiency vs. position along the ingots pulled from the same crucible.

2. Experimental

Two runs (Run A and B) of multiple mono-crystalline ingots (ϕ200mm) with a total weight of up to 800 kg pulled from a single crucible in a CCz puller were characterized. The ingots were doped by phosphorous to be n-type. All ingots from the Run A were characterized for MCLT, resistivity (R_s), interstitial oxygen (O_i) and substitutional carbon (C_s) previously [1]. Additional MCLT measurements were conducted on these ingots at different minority carrier density (MCD) using Sinton BLS-1 tester. The ingots from the Run B were characterized for MCLT both axially and radially. Ingots were then sliced into 156mm pseudo square wafers by slurry (Run A) as well as by diamond wire (Run B). Wafer surfaces were passivated by thin layers of a-Si film on both front and back sides before being characterized for R_s and MCLT using Sinton WTC-120 tester. Wafers from different ingots and different locations of selected ingots together with the reference Cz wafers were fabricated into HJT cells in ENN's HJT industrial pilot line. The cell process flow was, SDR → Texture → Clean → a-Si Deposition → TCO Deposition → Electrode Printing.