Microelectronics Reliability 55 (2015) 2607–2613

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/mr

Introductory invited paper

System efficient ESD design

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ARTICLE INFO

Article history:
Received 29 April 2014
Accepted 9 December 2014
Available online 29 October 2015

ABSTRACT

System-level ESD robustness is a crucial feature for any electronic system. To achieve the required level of robustness at the lowest cost a design concept is applied which assures matching between PCB protection components and IC IO behaviour under system ESD discharge. It is now widely referred to as system efficient ESD design (SEED).

A thorough characterization of the high current behaviour of IO circuit and on-board protection elements provides the necessary data for a simulation based co-design of on-chip and on-board protection measures. The constraints for characterization and modeling are discussed. Applying this methodology allows the development of a cost optimized system-level ESD protection throughout the stages of a system design.

1. Introduction

Electrostatic discharge (ESD) robustness of systems is one of the key concerns in the design of electronic systems [1,2]. Electrostatic discharges of various kinds are permanent companions when systems are operated by the end-customer. As electronic components are used in core functions of most vehicles and other safety relevant applications, the robustness against ESD is of utmost importance of the system [3,4].

There is a hierarchy of design measures ranging from on-chip protection circuits to the design of the system housing to implement ESD robustness [5,6]. Another standard that has been investigated is the cable discharge events (CBE) [7]. A trend in the industry is seen to shift the system robustness requirements to the single building block of the system like the IC, in the hope to facilitate the system design and to save costs. However, with growing performance requirements and shrinking technology dimensions, IC suppliers are less and less able to guarantee full system on-chip ESD robustness. Actually, such an approach is neither required nor efficient in most cases. It leads to immense overdesign for ICs even in less advanced technologies. Even further, achieving the system protection for an IC does not guarantee that it is effective for other applications of the same IC. Thus it is important to understand the principles of system protection from a new point of view than what has been the common practice. What is more important is to consider how the IC is implemented in the system board.

As it will be discussed in this paper, a good knowledge of the exposed pins and their careful characterization allows the implementation of consistent protection measures at the various stages of the system design [8]. Such a co-design approach is most efficient and cost-optimized. The purpose of the paper is to give an overview of this novel design methodology.

2. Miscorrelation of system level to on-chip ESD robustness

There is a prevalent misconception in the industry that a high HBM or CDM robustness of an IC guarantees the robustness of the system where the IC is assembled. First, the shapes of these waveforms from HBM and CDM to system level (IEC) are quite different as shown in Fig. 1 [9]. The HBM pulse is applied between two or more pins in an unpowered part. CDM is tested when static charge is built on an unpowered part and then discharged from a single pin to low resistance ground. Also, whereas HBM and CDM failures are based on physical damage, the system level failures can be based on system upset including physical damage. The discharge paths and current paths are distinctly different and therefore no correlation can be expected. Moreover, the IEC robustness requirement is based on 4 kV or 8 kV stress requirements which results in considerably higher stress currents compared to HBM stress at the same levels. For example, Fig. 2 illustrates this case for 4 kV stress where the IEC-Gun test is much harsher. The HBM/CDM stress tests are in contrast to the system level IEC test where in the latter the chip is mounted on the board and stress pulse is applied at various points on the system with reference to ground of the power supply. In this test power is often applied during the stress.

The widely spread opinion that ICs showing high HBM or CDM robustness level are easier to protect on board-level and need less on-board protection components, is misleading as long as the on-chip protection is not able to handle the complete IEC stress. Actually, there have been reported some systems that contain ICs with only 500 V HBM robustness but still passing 8 kV IEC [9]. In contrast, in some cases a design improvement of HBM level of ICs to beyond 2 kV HBM have been

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http://dx.doi.org/10.1016/j.microrel.2014.12.020
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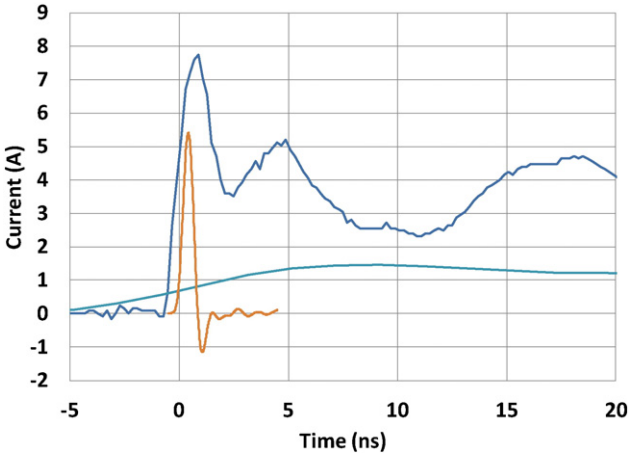

Fig. 1. Comparison of component versus system level ESD current waveforms. Courtesy of Robert Ashton.

recorded to cause a drop in the IEC robustness of the system [8]. Therefore it is concluded that system level ESD performance is not correlated to the component level ESD robustness. Assessing the mechanism of IC-level fail and system level fail in more detail, a number of differences can be detected. First, system level ESD is applied to powered systems and can address very different failure modes compared to HBM and CDM, which are applied to unpowered ICs. Low level IEC fails are often related to functional fails, which cannot occur or are detected in unpowered ICs. Also, the stressed circuit paths in powered and unpowered system can be very different (Fig. 3).

During IEC test the positive ESD pulse will be shunted to the VDD rail and buffered by the capacity of the on-board capacitors and the battery in the powered system, while in an HBM test the positive pulse to ground discharge has to trigger the breakdown protection elements to ground.

Fig. 3 also shows that the discharge path in the system is divided into on-chip and on-board branches. The resulting overall robustness of the system depends essentially on the ratio of the current in these branches which is determined by the switching behaviour of the devices and the resistance in the paths. For these reasons the IC-level HBM or CDM pass levels are not relevant to the system level protection design.

Apart from systematic differences between IC-level and IEC ESD test, IEC testing procedure itself introduces uncertainties, when different systems are compared. E.g. changing the ground return path or the ground plane in the test set-up, leads to very different results.

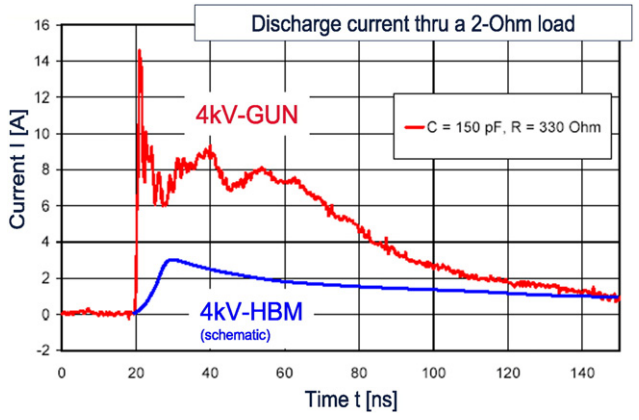

Fig. 2. Comparison stress current levels between 4 kV HBM and 4 kV IEC tests. Courtesy of Markus Mergens.

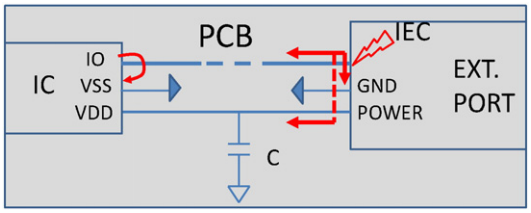

Fig. 3. During the IEC test if the system is powered the current paths can be different and the on-board capacitors will play a role.

In summary, these effects prevent from a general correlation between IC level and system level ESD pass levels, in special cases of HBM and CDM to IEC.

3. Overview/definition SEED

3.1. SEED concept

To clearly define this "System Efficient ESD Design" it is important first to understand the energy coupling that can take place between the external port, where the IEC system pulse is applied, and the interfacing IC pin. For this purpose we will assume that the system board offers an external (off-chip) protection with a transient voltage suppressor (TVS) device. Naturally, the TVS device is expected to dissipate the major brunt of the high current pulse, but some portion of it will spill into the IC pin discharging (to ground) through its component ESD cell. This is referred to as the "Residual Pulse." [10]. The next step is to understand what factors determine the residual pulse and when the IEC pulse is applied how much of the energy is transferred to the IC pin.

The above is illustrated in Fig. 4 when the IEC pulse is applied at the external port [9]. The major current path is through the TVS device. Combined with this, the printed circuit board (PCB) design essentially determines the residual current going into the IC pin. This path impedance consists of the trace resistance and inductance, and board elements such as the common model filter (CMF) or the chip ferrites (CF). With the IEC pulse applied although the TVS turns on at a lower voltage (typically 6 to 7 V) the on-resistance of this device rises the voltage to nearly 40 to 50 V due to the high discharge current level of the IEC pulse. Then the voltage difference between the TVS device and the ESD clamping device along with the PCB resistance will determine the final residual current [10]. Thus, lower the clamping voltage of the on-chip ESD device and combined with a lower on-resistance will require higher amount of PCB resistance. A careful simulation approach [11] can be modeled to design the proper required PCB resistance. Although this is a simple approach for designing to avoid hard failures, the actual simulations taking into account the desired frequency response of the components is necessary for effective system function. One such example for the USB2 design was recently reported [12]. The importance of simulating the residual current is illustrated in Fig. 5. The failing limits from 100-ns characterization of the USB pins are indicated in the figure.

In Fig. 5, from the "PCB with no TVS" curve it is obvious that a TVS device is essential to protect any interface pin. Next from the "TVS Only"

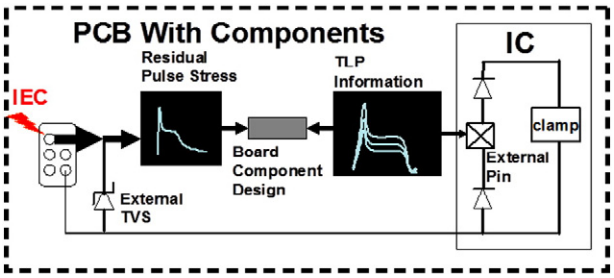

Fig. 4. The concept of residual pulse after IEC stress is applied at the external port.