

# Heavy-ion irradiation study in SOI-based and bulk-based junctionless FinFETs using 3D-TCAD simulation

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## ABSTRACT

In this paper, SOI-based and bulk-based junctionless FinFETs subjected to heavy-ion irradiation are scrutinized using 3D-TCAD simulation. Since the junctionless devices need heavy doping concentrations, devices with various fin dopings are studied for their radiation performance. Transient drain current device simulations depict higher disturbances in bulk devices. Bipolar amplification is higher in SOI devices. The soft error performances of the SRAM cells based on the above devices are also explored. Even though the SOI devices have higher bipolar amplification than the bulk device, they show better soft error performance in SRAMs.

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## 1. Introduction

In the CMOS evolution, junction less devices are the younger devices that have no junction and contain single doping species at same level in its source, drain and channel region. They are bulk conduction devices where the current transport is in the bulk of the semiconductor, which enhances the mobility in ON-state and reduces the impact of imperfect semiconductor/insulator interfaces [1–6].

Junctionless (JL) devices even though introduced on SOI substrate, bulk-based junctionless devices are also investigated. A comparison study between SOI and bulk based junctionless devices (SOI JL and Bulk JL), based on DC performance metrics, is available in [5]. The heavy ion irradiation simulation study by Daniela Munteanu et al. [7] compares the junctionless device with the inversion mode device. It is reported that the large floating body effects in junctionless devices reduce the device immunity to Single Event Upset (SEU).

On one hand, the reduction in the sensitive charge collection volume is a positive aspect of the SOI technology. But on the other hand, the increased bipolar amplification in SOI reduces the SEU (Single Event Upset) hardness [8]. In essence, the impact of radiation is a concern in

bulk as well as SOI devices [9]. A radiation study between SOI and bulk based conventional FinFET devices has been explored [10]. A comparison study between SOI and bulk based junctionless devices, with respect to irradiation, is yet to be studied. The results/conclusions derived at the device level studies may not be applicable at the circuit level. Coming to circuit level soft error or single event upset (SEU) is a temporary failure that occurs in SRAM circuits as a result of high energetic particle strike. As we scaled down the devices soft error rates are projected to increase [11].

This work has two parts (i) Studying drain current perturbations during radiation and calculating bipolar gains in bulk JL and SOI JL devices and (ii) Studying soft error performance of the bulk JL and SOI JL-based SRAMs. All the studies are done using 3-D TCAD simulations. The paper is organized as follows: Section 2 provides device structure and  $I_D$ - $V_G$  calibration, Section 3 provides simulation results and discussions. The conclusion is explained in Section 4.

## 2. Device structure and $I_D$ - $V_G$ calibration

Sentaurus TCAD simulator from Synopsys is used for this study. The simulator has many facilities and the following modules are used in this study.

- Sentaurus Structure Editor (SDE): To create the device structure, to define doping, to define contacts and to generate mesh for device simulation.

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- Sentaurus Device Simulator (SDEVICE): To perform DC and transient simulations.
- SVisual and Inspect: To view the results.

The schematic structure of N-type Junctionless FinFET is given in Fig. 1(a), (b) and (c). The structure generated from SDE for n-type bulk JL and SOI JL is shown in Fig. 2(a) and (b) respectively. For better view, 2D cutline of the device structure is depicted in Fig. 3. The parameters considered for these devices are given in Table 1. The models used in the device simulation include Auger recombination model, SRH recombination model with carrier lifetimes depending on the doping level as well as the Fermi–Dirac carrier statistics, doping dependent mobility model, and field dependent mobility model. Quantum corrections are also taken into account. The default parameters of the simulator are tuned to match the drain current ( $I_D$ ) versus gate voltage ( $V_G$ ) characteristics against the published results [5] and is shown in Fig. 4(a). The high-k spacer ( $\text{Si}_3\text{N}_4$  spacer) is used to further optimize the device performance [6] and is given in Fig. 4(b).

Three fin doping levels have been considered in simulation:  $1 \times 10^{19} \text{ cm}^{-3}$ ,  $1.5 \times 10^{19} \text{ cm}^{-3}$  and  $2 \times 10^{19} \text{ cm}^{-3}$ . To have a fair comparison among bulk and SOI devices gate work function are finely tuned to obtain the same off state current ( $I_{\text{OFF}}$ ).

Fig. 4(a) and (b) show the ‘without spacer  $I_D$ – $V_G$ ’ and ‘with spacer  $I_D$ – $V_G$ ’ respectively, for bulk and SOI based junctionless devices used in this study, for a fin doping of  $1.5 \times 10^{19} \text{ cm}^{-3}$ . When we introduced

the spacer as a mean to enhance the device performance, we have also changed the gate electrode work function to achieve the same  $I_{\text{OFF}}$  for both bulk and SOI devices. As already stated this was done for fair comparison. It can be noticed from Fig. 4(b) that both the SOI and bulk devices have the same  $I_{\text{OFF}}$ .

### 3. Results and discussions

The radiation strike is simulated using the heavy ion models in SDEVICE [12]. The electron–hole pair column created in the device by the ion strike is modelled using a carrier-generation function which has a Gaussian radial distribution with the characteristic radius of 20 nm. The time distribution of ion track has a Gaussian shape centred at 25 ps and with a characteristic width of 2 ps [7].

At device level radiation study, off state drain current perturbation and bipolar amplification are taken as performance metrics. At circuit i.e. SRAM level, the critical radiation dose ( $\text{LET}_{\text{th}}$ ), minimum dose required to flip the cell contents, is used as a metric to study the soft error performance.

#### 3.1. Impact of radiation on bulk JL and SOI JL devices

Biasing the device in off-state with  $V_G = 0 \text{ V}$  and  $V_{\text{DD}} = 1 \text{ V}$ , the radiation strike is initiated. A radiation dose of,  $\text{LET} = 1 \text{ MeV}/(\text{mg}/\text{cm}^2)$  is

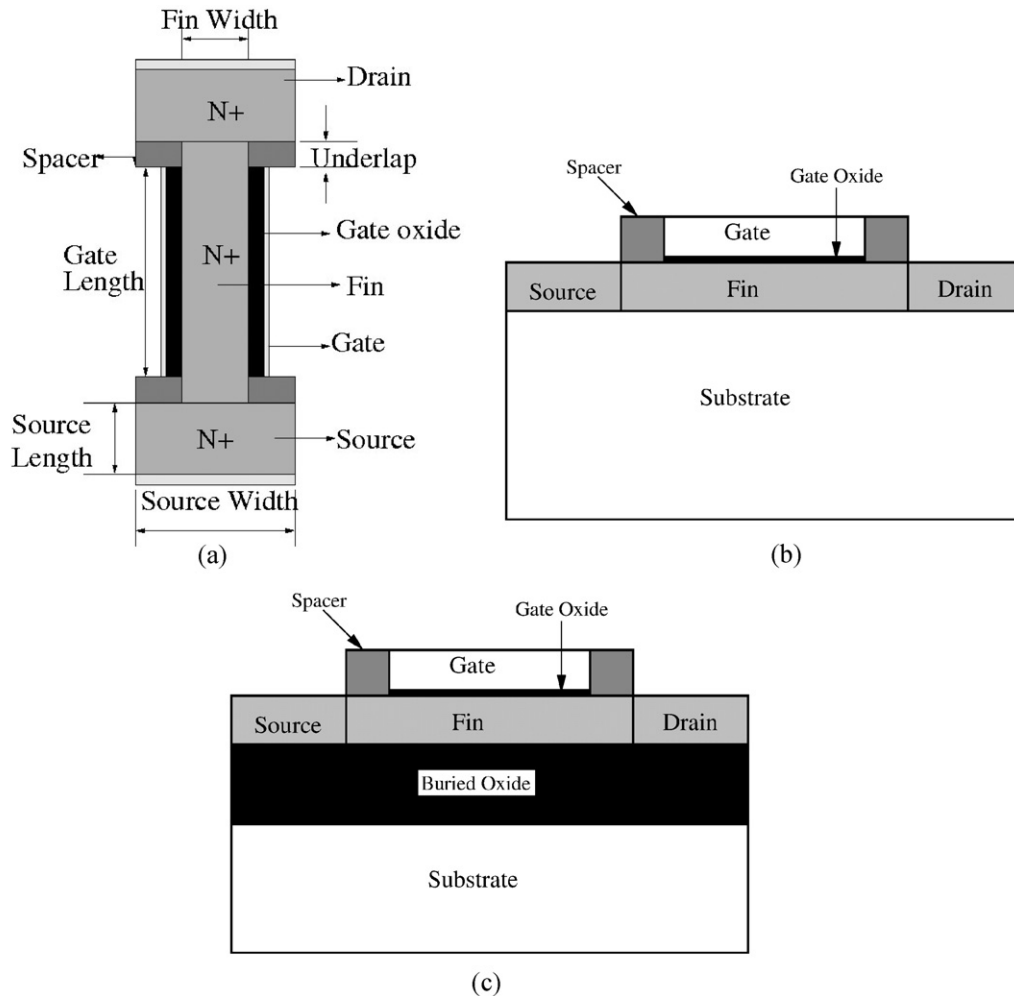


Fig. 1. (a) Schematic of the top view of junctionless device along xy plane. (b) Schematic of the side view of bulk junctionless device along yz plane. (c) Schematic of the side view of SOI junctionless device along yz plane.

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