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AlN capping layer inserted between Cu and SiCN dielectric barrier layer for enhancing reliability of 28 nm technological node and beyond

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ABSTRACT

The improvement of the interface adhesion between Cu and silicon carbonitride (SiCN) dielectric barrier layer is required in the back end of the line for 28 nm technological node and beyond. The main purpose of this paper was to investigate the reliability of breakdown voltage (VBD) and electromigration (EM) improved by inserting the AlN capping layer enhancing the above mentioned interfacial adhesion. The AlN capping layer was deposited by the ALD process using trimethylaluminum and ammonia precursors. The AlN capping layer was characterized by a cross-sectional transmission electron microscopy (XTEM) and energy dispersive X-ray spectrum (EDX) for the thickness and interfacial composition, electrical test for resistance–capacitance examination, reliability test for VBD and EM lifetime. XTEM observation indicated that the thickness of the AlN capping layer was about 8.5 nm, and the EDX examination indicated the Al and N elements of the AlN capping layer were distributed in the interface between Cu and SiCN dielectric barrier layer. Reliability test indicated that the VBD and EM performances were improved obviously by inserting the AlN capping layer for enhancing the interfacial adhesion between Cu and SiCN dielectric barrier layer.

1. Introduction

Cu as an interconnection metal material has been widely used in ultra large-scale integrated (ULSI) circuits. As the feature size of the device is scaling down from one node to the next, the main challenge associated with scaling down interconnection wiring is the improvement of the resistance capacitance (RC) performance in the precondition of the undegrade yield and reliability [1].

At present, the Cu interconnection is fabricated using the damascene structure. The Cu interconnection is formed by depositing a dielectric layer on a planar surface, patterning it using photolithography and dry & wet etch, then filling the recesses with Cu. The excess Cu is removed by chemical mechanical polishing (CMP), while the troughs or channels remain filled with Cu. After the CMP process, the Cu surface is exposed in the atmosphere to be easily oxidized at low temperatures (<200 °C) in a typical processing environment. Furthermore, Cu cannot form a stable self-limiting surface oxide layer like W and Al, and its oxide is chemically and mechanically unstable., Therefore, the Cu oxide presented on the surface of the Cu causes the two aspects of the problems: (1) Cu oxide can affect adversely the adhesion of Cu to adjacent passivation, barrier, and protective cladding layer. (2) The Cu oxide has a higher resistivity than pure Cu, which causes the increase of the overall resistivity of the interconnection and the problem of the device reliability [2–4].

A number of recipes are used for removing Cu oxides, such as sulfuric acid wet etching, thermal treatment in vacuum at 350 °C, hydrogen (H_2) plasma treatment, and ammonia (NH_3) plasma treatment [4–6]. After the above mentioned pretreating process, a diffusion dielectric barrier film (SiN, SiC), or silicon carbonitride (SiCN) is required to deposit on Cu metallization for blocking Cu diffusion. The dielectric barrier film is capped on the surface of the Cu to improve effectively electromigration (EM) lifetime as the device size becomes small and the current density through the interconnection becomes high [7–13].

For the conventional structure of Cu interconnection, TaN/Ta or other barrier metals are covered on the side and bottom before Cu filling, and SiCN dielectric barrier layer is capped on the top of the Cu. The problem is that the adhesion of Cu to dielectric barrier film is lower than that of Cu to metal barrier layer, and the Cu atoms are prone to diffuse from the top of the interconnection. This causes the voids in the Cu interconnection wiring to result in the device failure and reliability problem, which is solved using a self-aligned metal cap before the dielectric barrier layer deposition [14–16].

Kang reported [17] that a silver (Ag) capping layer was used for a metal barrier to prevent the formation of Cu oxide after the CMP process. In order to simplify process step, the Ag barrier during the CMP process was in situ formed using the displacement reaction at either the second step of Cu CMP or the buffing step. Yang reported [18] that the Co was deposited selectively on the Cu surface by optimizing process such as raising deposition pressure and adopting a pre-clean process prior to the Co deposition, which was not deposited on the dielectric film surface. The thickness of Co cap layer was 6 nm, which

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made the EM lifetime present significant improvement. Furthermore, self-aligned metal capping layers formed by electroless plating, such as CoWP (cobalt tungsten phosphorus) and NiMoP (nickel molybdenum phosphorus), are investigated in a number of Cu interconnection technologies. One application is in high performance logic chips of the 45 nm node and beyond [19,20]. The self-aligned W capping layer with good selectivity is obtained by chemical vapor deposition (CVD). The isolation resistance and leakage current between adjacent Cu interconnection capped by W are similar to those between conventional Cu interconnection. The, self-aligned capping layers of W or cobalt tungsten boron are applied to suppress the stress-induced void in Cu interconnection [21]. A self-aligned Mn capping layer using CVD process is introduced to strengthen the interface between Cu and dielectric film, which does not cause the increase of Cu resistivity [22].

However, the weak adhesion between Cu and the dielectric capping layer can cause rapidly electromigration failure of the Cu interconnection. AlN is in possession of excellent properties such as superior dielectric strength (140 to 170 kV/cm) and good thermal conductivity (90 W/m °C), which is a potential material for improved performance of the Cu interconnection in recent year [22]. The main purpose of this paper was to investigate the electric properties and reliability of the AlN film capped on the surface of Cu after the CMP process for 28 nm technology node and beyond. The cross-sectional transmission electron microscope (XTEM) and energy dispersive x-ray spectroscopy (EDX) were used to examine element distribution in the interfaces among Cu/AlN capping layer/SiCN dielectric barrier layer. The model of AlN capping layer to enhance interfacial adhesion was set up to understand the voltage breakdown (VBD) and EM reliability to be improved.

2. Experimental

For the integration circuit, Cu interconnection in the back end of the line (BEOL) was fabricated using the damascene process. With feature size of the device scaled down 28 nm technological node and beyond, the insulator used in the interlayer level of the BEOL was SiOCH porous ultra low k (p-ULK) film with dielectric constant of ~2.55. All dielectric films were deposited on the 300 mm wafer using a plasma enhanced chemical vapor deposition (PECVD) process. The integration scheme of the BEOL was "trench-first and via-next" approach to fabricate dual damascene structure. The hardmasks of three layers were TiN, oxide, and low k film, respectively.

The AlN capping layer was directly deposited on the surface of Cu after CMP process and before SiCN dielectric barrier layer deposition. The film stack was TiN/oxide/low k film/p-ULK/SiCN/AlN/Cu. Fig. 1 depicted a schematic cross-section of the dual damascene metallization. The p-ULK films were deposited on 12-inch p-type silicon wafer by two step sequence. Firstly, the SiOCH film was co-deposited by PECVD at a temperature of 260 °C using diethoxymethylsilane (DEMS) precursor as a network matrix and alpha-terpinene (ATRP) precursor as the sacrificial porogen. The PECVD system using the parallel plate was manufactured by Applied Materials Inc. (AMAT). The ratio of the ATRP flow to DEMS flow was 1.5:1–1.7:1. The DEMS and ATRP precursors were introduced into chamber using the He carrier gas. Subsequently, the above co-deposited SiOCH films were exposed to UV radiation with wavelength ranging 200 nm–400 nm at 385 °C about 120–240 min. The porogens were removed from the matrix and the pores were remained, which formed the p-ULK film.

TiN metal hard mask layer with thickness 200–300 Å was deposited in AMAT tool using physical vapor deposition (PVD) process. Tetraethyl orthosilicate (TEOS) hard mask with thickness 100–200 Å was deposited in AMAT producer SE tool using the PECVD process at 400 °C, and the precursors were the TEOS and oxygen. Dense low k used as dielectric hard mask layer with thickness ranging 100–200 Å was deposited in AMAT producer SE tool using the PECVD process at 350 °C, and the precursor was octamethylcyclotetrasiloxane.

AlN capping layer was deposited by an atomic layer deposition (ALD) process in Lam research tool using trimethylaluminum (TMA) and ammonia precursors [23]. Subsequently, the SiCN dielectric barrier layer was deposited on the AlN capping layer. The PECVD process was used for depositing SiCN film using Lam research tool at 350 °C, and the precursors were tetramethylsilane (4MS) and ammonia. The interfaces among Cu, AlN capping layer, and SiCN dielectric barrier layer were observed by the XTEM, and the compositions in the interface were analyzed by the EDX. The capacitance and resistance test were carried out using a standard meter in a shielded probe station at room temperature.

VBD reliability test was probed on a combed type test structure comprised of three layer Cu and one top layer Al interconnection. Reliability performance of the AlN capping layer combined with SiCN dielectric barrier layer was investigated by ramp-voltage test where the leakage current between metal 2 lines in interspersed combs was measured with increasing applied electrical voltage at a constant ramp rate of 1 V/s. As the wafer level package was completed, EM lifetime test was carried out at 300 °C with an electrical current density of 1.25 MA/cm^2. The resistance increases to 10%, which was used as a failure criterion for the EM test.

3. Results and discussion

3.1. XTEM micrograph and EDX analysis

In order to examine the AlN capping layer deposited by the ALD process, the XTEM is used for observing the physical property of the AlN capping layer, and the elemental mapping of the AlN capping layer is analyzed using the EDX. Fig. 2 shows XTEM micrograph (a) and the elemental mapping of the EDX (b) without AlN capping layer. As shown in Fig. 2(a), XTEM micrograph indicates that the thickness of the SiCN dielectric barrier layer is about 20 nm when it is directly deposited on the surface of the Cu. Fig. 2 shows the mappings of Ta + Si, Ta, N, Cu, and O elements using the EDX examination. The Ta + Si and Ta elements are distributed on the sidewall of the Cu line, corresponding to red mapping and green mapping of the EDX. The pink mapping of the EDX corresponding to the N element indicates that SiCN film is capped

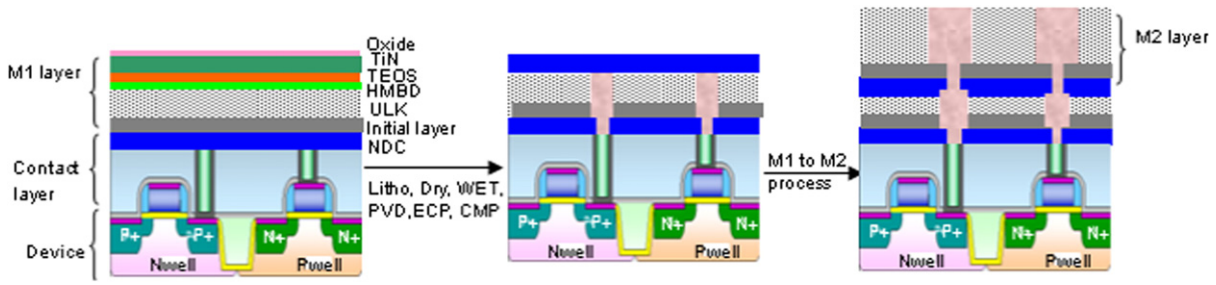

Fig. 1. Schematic cross section of 28 nm node BEOL interconnect configuration.