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Inverse Gaussian distribution based timing analysis of Sub-threshold CMOS circuits

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ABSTRACT

Aggressive technology scaling and ultra low power constraints have resulted in less predictable device behavior complicating timing analysis/estimation. The traditional delay models fail to accurately capture the circuit behavior under such conditions. This paper proposes a novel highly accurate Inverse Gaussian Distribution (IGD) based delay model applicable to both combinational and sequential elements for sub-powered circuits. The IGD based delay estimation accuracy is demonstrated by evaluating multiple circuits, i.e., D Flip Flops (DFFs) + 8-bit Ripple Carry Adder, and 8-bit De-multiplexer (DEMUX) and Multiplexer (MUX). Our experiments indicate that the IGD based approach provides a high matching against HSPICE Monte Carlo simulation results, with an average error less than 1.9% and 1.2% for the two circuits, respectively, while sparing orders of magnitude simulation time. Moreover, the IGD model outperforms the traditional Gaussian Distribution (GD) model by providing 6× better average accuracy with no extra simulation time overhead.

1. Introduction

Successful timing analysis is the method of computing the maximum clock frequency at which the circuit can safely operate thereby guaranteeing the correct chip functionality post fabrication. Accurate yet efficient timing estimation models are desirable for the evaluation of digital IC's performance. With the continuous scaling of the transistors, the impact of process variations and voltage scaling has resulted in challenging the timing analysis. Unpredictable gate delay values induced by local variations [1] along with other variations like CMOS channel length, threshold voltage, and oxide thickness are some of the key factors that complicate timing analysis and estimation [2]. Further, with the introduction of sub-threshold logic [3], the CMOS circuits supply voltage value has been pushed to an extremely low level, which is near or below the MOSFET threshold voltage. This dramatically reduces the power consumption but aggravates the process variations there by compromising circuit functional performance [4]. Hence, accurate delay analysis and estimation is turning out to be even more challenging and the capabilities of conventional delay models and timing analysis approaches are proving to be inadequate.

Traditional approach is to perform highly accurate SPICE simulations with the downside being the inevitable long runtimes. To overcome this, corner analysis has been widely adopted and deals with multiple Process, Voltage, and Temperature (PVT) corners. However, the high sensitivity and unpredictability of deep submicron CMOS devices turns this approach to being either overly pessimistic or optimistic [5]. Several improved methodologies have been proposed to achieve better accuracy within acceptable computing time. Statistical Static Timing Analysis (SSTA) [6] was proposed to determine the distribution of propagation delays and signal timing violation on digital CMOS circuit critical paths. Nonetheless, SSTA requires burdensome efforts to automate the approach while disregarding the input pattern delay dependence. In order to overcome these obstacles, Monte Carlo Static Timing Analysis (MCSTA) [6] and Dynamic Timing Analysis (DTA) [7] were proposed. The MCSTA is the one-off generation of a Variation Cell Library for standard cells, which is used to carry out static timing analysis to create thousands of randomized gate-level net-lists. MCSTA can be considered as a trade-off between the time consuming Monte Carlo (MC) SPICE simulation and the relatively inaccurate SSTA. A statistical DTA approach that employs the normal Gaussian approximation to model the propagation delay on the basis of distinguishable input patterns was presented in [8]. While reasonably accurate, the approach can be costly in terms of processing time, as its accuracy directly depends on the number of considered input vectors.

In this paper, a comprehensive delay approximation methodology based on Inverse Gaussian Distribution (IGD) is proposed. We introduced the primitive version of this model in [9] applicable to combinational elements in digital CMOS circuits to compute key parameters of the model. The main idea behind the proposal is to first gather the basic gate key parameters by means of MC simulations and then linearly extrapolate (propagate) them through the logic network at the circuit level. In this refined approach, the effect of fan-out value and input transition time on the gate delay is also taken into consideration. Moreover, the model is extended to cover sequential components as well. The

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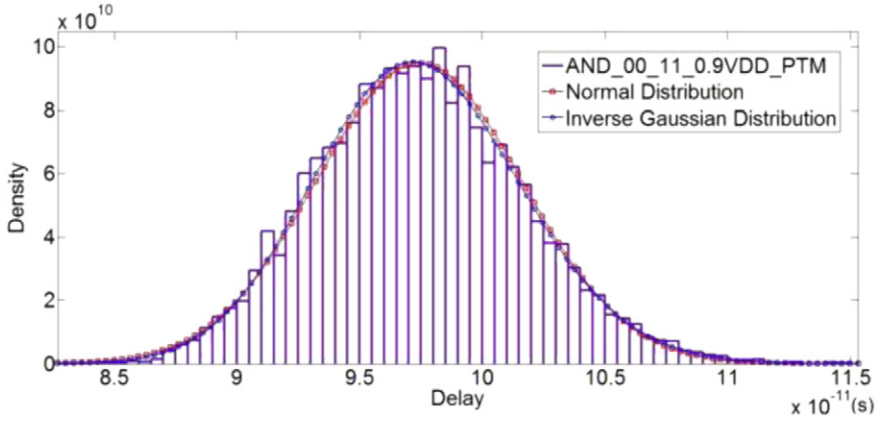

Fig. 1. IGD vs GD approximation for 2-input AND gate @0.9 V V_{dd}.

proposed IGD model is endorsed by physical phenomena and provides considerable delay estimation accuracy and efficiency. Furthermore, the model is highly accurate even for different power supply voltage values ranging from nominal V_{dd} to sub-threshold V_{dd}. This approach is significantly faster than the state-of-the-art since only the basic cells have to be fully simulated in order to obtain the key model parameters and the delay model for complex circuits. Unlike other techniques or tools, which demand large look-up tables or complicated calculations [6,7], the proposed approach is remarkably straightforward.

To demonstrate the practicability of the IGD based statistical approach, we compared the estimated delay with the current model and MC SPICE simulations for several combinational and sequential logic blocks. 32 nm technology models were employed across all the simulations. Experimental results indicate that the proposed method outperforms GD fitting and provides a very close match with MC simulations, i.e., less than 1.2% and 1.9% error for the two considered circuits. For the simulation set-up, process variations and voltage variations are investigated during this key-parameters estimation step. Temperature variation is not taken into consideration due to not only its less significance compared with the aforementioned two parameters but also the temperature inversion effect (in sub-threshold region, also known as weak-inversion region, the higher the temperature the smaller the propagation delay), thereby the room temperature is chosen for all the simulations [3].

The rest of the paper is organized as follows. In Section 2, the IGD delay model is introduced and collated with other related work to demonstrate its accuracy and flexibility. Then, in Section 3, IGD models and their key parameters for combinational and sequential CMOS elements are presented. After that, the IGD model expansion to capture the fan-out and input transition time, effects is explored in Section 4. Thereafter, the delay estimation approach is applied in Section 5 on two circuits: (i) DFFs + 8-bit Ripple Carry Adder (RCA) and (ii) DFFs + 8-bit De-multiplexer (DEMUX) and Multiplexer (MUX). Finally, conclusions and future work are discussed in Section 6.

2. Inverse Gaussian Delay model

In this section, comprehensive delay approximation methodology based on Inverse Gaussian Distribution (IGD) is introduced. We first introduce the IGD model and compare with other related work namely, the Gaussian Distribution (GD) delay model [8]. The proposed IGD delay model behavior is then explained with theoretical endorsement. To demonstrate the accuracy and flexibility of our approach, both conventional V_{dd} and near/sub-threshold V_{dd} values in conjunction with different types of process variations are considered.

A. Related work

A propagation delay estimation algorithm [8] based on GD was employed to compute delay, where a close match was found between the measured propagation delay profile and the Gaussian Probability Density Function (PDF). However, the choice for approximating the delay PDF with a normal distribution was based on fitting only two Monte Carlo simulations with no scientific explanation to support the model. Although the GD delay model matches closely under nominal voltage supply, several GD characteristics hint its inability to capture delay data distributions in the general case. First, by definition, GD is characterized by a function with the field of real numbers as its support, which indicates that it assumes non-zero value also for negative time values. This is a clear mismatch with the circuit physical reality since

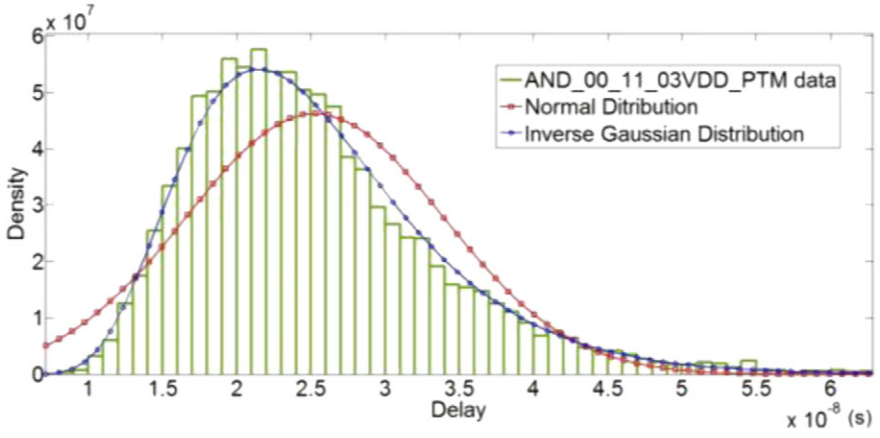

Fig. 2. IGD vs GD approximation for 2-input AND gate @0.3 V V_{dd}.