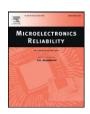
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Using RBF networks for detection and prediction of flip chip with missing bumps



Guanglan Liao ^a, Li Du ^{a,*}, Lei Su ^a, Miao Zeng ^a, Lei Nie ^b, Tielin Shi ^a

- a State Key Laboratory of Digital Manufacturing Equipment and Technology, Huazhong University of Science and Technology, Wuhan 430074, China
- ^b School of Mechanical Engineering, Hubei University of Technology, Wuhan 430068, China

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ABSTRACT

Flip chip has been extensively used in microelectronic packaging industry. With the trend of solder bumps towards small volume and ultra-fine pitch, defect inspection of flip chips has become more difficult. In this work, we introduce radial basis function networks for detecting and predicting missing solder bumps, a typical defect in flip chips. Eight time and frequency domain features extracted from the flip chip vibration data are inputted to the networks, and flip chips with missing bumps distributed adjacently or randomly are detected and predicted. For the PAC2.1 flip chips with missing bumps distributed adjacently, we distinguish the defective flip chips from the reference one with a 100% accuracy. The flip chips with 1 to 2 missing solder bumps are then trained and detected accurately by the network, and the chip with 3 missing bumps can be predicted exactly as well. After that, we train the network with the data of flip chips with 1 to 4 missing bumps. The network can recognize the number of the missing bumps in these flip chips with a 100% accuracy, and predict 5 missing bumps in the flip chip with the accuracy of 91.7%. For further validation, we use the PBO8 flip chips with missing bumps distributed adjacently or randomly for training, testing and prediction, and also obtain high accuracies. These prove the feasibility of using RBF networks for detection and prediction of flip chips with missing bumps in engineering.

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1. Introduction

Flip chip technology is a key driver for high density packaging and complex system integration [1–5]. Small solder bumps are arranged between the chip and substrate, providing superior electrical connection and thermal conduction. Meanwhile, it is critical and difficult to detect high-density small solder bumps in flip chips [6-8]. Open and cracked solder bumps can sometimes be found using electrical testing method, however, the partial cracks and cold bumps that provide only an intermittent electrical connection would be passed [9]. X-ray radiography is a useful approach for detecting solder bump voids, bridging and other physical abnormality, whereas it is hardly to detect fine cracks and delaminations. X-ray laminography and tomography are effective 3-D techniques for inspecting complex flip chip defects [10-12], while the prohibitive equipment costs prevent the techniques from being widely used. Scanning acoustic microscopy (SAM) utilizes high frequency propagating ultrasonic waves through the sample to examine internal conditions of the component. The reflected ultrasonic waves can indicate poor adhesion and voids [13-15]. When defects occur in the periphery of the chips, the edge effect may affect detection accuracy. Moreover, the liquid couplant used during the measurement may bring damage to the chips. Recently, flip chip inspection method based on vibration analysis has been introduced [16–18]. It is a nondestructive and fast approach that can be used for online inspection.

Artificial neural network (ANN) has increasingly been applied for signal processing in many fields [19,20]. The network can be viewed as performing a curve-fitting operation in a multidimensional space [21] and is proved to be an attractive method of solving pattern recognition and fault classification issues [22]. Radial basis function (RBF) network, one kind of feedforward networks, has advantages of simple structure, self-adapting architecture determination [23] and quick convergence speed [24]. In this paper, vibration analysis together with RBF networks were introduced for detection and prediction of flip chips with missing solder bumps. A laser scanning vibrometer was employed to capture the flip chip vibration signals, and eight time and frequency domain feature parameters were extracted from the vibration data. Then RBF networks were constructed, the features of the flip chips were inputted to the network for training and diagnosing, and high accuracies were obtained.

2. Flip chip defect inspection

The inspection of flip chips with missing bumps mainly includes three steps: vibration signals acquisition, feature extraction from the vibration signals and recognition of flip chips with missing bumps using RBF networks.

^{*} Corresponding author. E-mail address: li_du@hust.edu.cn (L. Du).

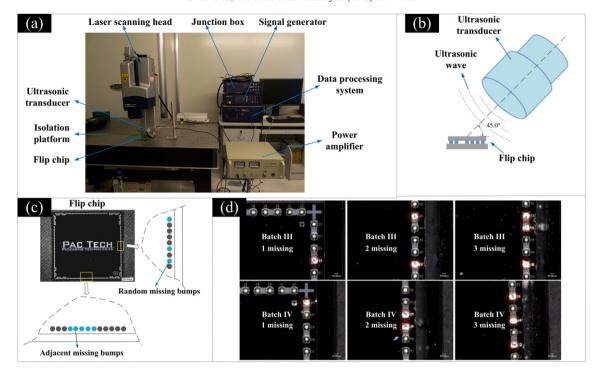


Fig. 1. (a) The experimental system. (b) The schematic diagram of the ultrasonic transducer and the flip chip. (c) The magnified schematic diagram of the flip chips with missing bumps distributed adjacently or randomly. (d) The positions of the randomly distributed missing bumps for the six PB08 flip chips from batch III and batch IV.

2.1. Vibration signals acquisition

The experimental system for flip chip defect inspection is shown in Fig. 1. A signal generator (Polytec, GEN-M2) is utilized to produce a continuous linear scan periodic signal as the excitation source since it has a wide bandwidth compared to the traditional sine voltage signal, as depicted in Fig. 2. The frequency band of the signal is 0–500 KHz, where the direct current component is filtered and the zero drift is suppressed. After magnified by a power amplifier (NJFNKJ, HFVA-62), the excitation signal is converted to ultrasonic waves by an air-coupled

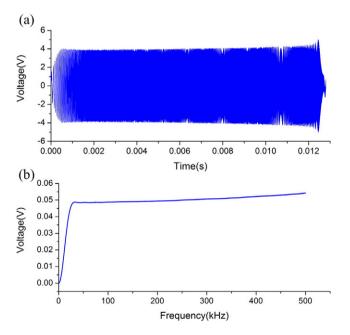


Fig. 2. (a) The time domain of the excitation signal. (b) The frequency domain of the excitation signal.

capacitive ultrasonic transducer (ULTRAN Group, CAP3) to excite the flip chips. The incidence angle from the transducer to the center of the flip chip surface is 45° (Fig. 1b). The vibration velocities of flip chips are captured by a laser scanning vibrometer (Polytec, PSV400) with a sample frequency of 1.28 MHz, where the scanning head has a spot size of 13 μm and the laser scanning vibrometer has a velocity resolution of 0.02 $\mu m/s$.

Generally, abundant data are beneficial for neural network training, recognition and prediction. Here two types of daisy-chain flip chips (Pac Tech, PAC2.1-PB184-200-10 mm and PB08-200 \times 200) are selected for verifying the method in detecting flip chips with missing bumps. The size of the PAC2.1 flip chips is $10\times 10\times 0.5$ mm, each having 46×4 solder bumps distributed evenly along the edges. The diameter and pitch of the bumps are $130~\mu m$ and $200~\mu m$, respectively. The size of the PB08 flip chips is $5.08\times 5.08\times 0.5$ mm and every chip has 22×4 solder bumps distributed evenly along the edges, where the diameter of the bumps is $120~\mu m$ and the pitch is $203~\mu m$. To introduce missing solder bumps in flip chips, we remove specific solder bumps manually by using fine-tipped tweezers with the assist of an image instrument (MC001-YR2010) before packaging. Then the defective chips are bonded to substrates by reflow soldering process without underfill.

The flip chips with no defects are used as reference chips, and the chips with missing solder bumps distributed adjacently or randomly are diagnosed, as denoted schematically in the zoomed view in Fig. 1c. There are six PAC2.1 flip chips (one reference chip and five chips with one to five missing bumps distributed adjacently), seven PB08 flip chips from two batches (batch I has five chips including one reference chip and four chips with one to four missing bumps distributed adjacently; batch II has two chips with one or three missing bumps distributed adjacently), and six PB08 flip chips from two batches (batches III and IV both have three chips with one to three missing bumps distributed randomly, where the optical images of the exact positions of these randomly distributed missing bumps are shown in Fig. 1d). We fix one flip chip with missing bumps on the isolation platform, locate spots on the edges of the flip chip, measure the vibration signals of these spots, and select the spot that has a relatively high response to the excitation. Then, we locate the scanning spot at the corresponding

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