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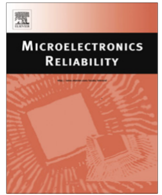

Investigation of geometry dependence on MOSFET linearity in the impact ionization region using Volterra series

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ABSTRACT

In this paper, investigation of device geometry on intermodulation distortion (IMD) of metal–oxide–semi conductor field-effect transistors (MOSFETs) is presented in the impact ionization region based on the Volterra analysis. As the gate length or gate width decreases, observed linearity improvement of the MOSFET in the breakdown regime is attributed to the more obvious breakdown inductance nonlinearity which cancels the transconductance nonlinearity. Linearity of the MOSFETs can be improved by choosing suitable device geometry in the breakdown region. It is believed the presented analysis results can benefit the reliability investigation for MOSFET linearity in the breakdown region.

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1. Introduction

Intermodulation distortion (IMD) analysis of metal–oxide–semi conductor field–effect transistors (MOSFETs) is essential to CMOS radio-frequency (RF) circuits because nonlinearities of a device can lead to degradation of linearity performance. IMD of a MOSFET is primarily resulted from the nonlinearity of transconductance and output conductance in the saturation region [1–3]. When gate length [4] is shortened in order to obtain better power gain and cutoff frequency, linearity performance of MOSFETs will decrease [5]. In addition, linearity performance of a MOSFET can also be dependent on the device gate width [5]. Therefore, the device geometry is an important parameter for the RF characteristic analysis of the MOSFETs [4–7].

The MOSFETs with shorter gate length can lead to impact-ionization induced avalanche breakdown [8,9] due to the high lateral electric field at the drain end of the channel. This high field effect is important for reliability issues [8,10] because the influence of MOSFET degradation on CMOS circuits due to an impact ionization effect can be a concern. Conventionally, direct-current (DC) measurements are employed to extract DC characteristics of the avalanche effects [11]. However, when the impact ionization effect is initiated, inductive impedance at RF can occur in the high field region [12], in addition to increased DC current. Device output characteristics at low gigahertz frequencies below 10 GHz [12,13] can be influenced by this RF impact ionization effect. For nonlinear characteristics, the RF breakdown mechanism can be bias-dependent [12,14], resulting in nonlinear distortion. Because the RF characteristics can be influenced by device geometry, understanding of the geometry impact on IMD characteristics is required to provide device information for CMOS high-linearity circuit designs with scaled-down MOSFETs.

Our previous research was focused on the MOSFET small-signal modeling in the breakdown region [12,15] and the mixed breakdown characterization for the p–n diode [16–18]. Another work investigated bias dependent IMD of MOSFETs in the avalanche region [14]. In this paper, we extend to the analysis of device geometry on IMD characteristics for MOSFETs in the breakdown regime through the Volterra series. Shorter gate length and narrower total gate width can improve the linearity of the MOSFETs in the avalanche breakdown region. The presented analysis results with respect to device geometry can benefit the reliability investigation for MOSFET linearity in the breakdown region.

2. Nonlinear characterization of the MOSFETs with different device geometry in the inductive breakdown region

The study of device breakdown behavior is important for circuit reliability evaluation as indicated in Ref. [19]. We infer that the

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MOSFETs operating in the breakdown region may bring a reliability issue due to high electric field Refs. [9,19] when compared with the normal operation. IMD is an important characteristic for device analysis and circuit design [1–3]. Therefore, the presented work focuses on IMD analysis in the RF avalanche region where inductive behavior occurs Refs. [12,15] to understand whether the breakdown operation is reliable or not. The nonlinear equivalent circuit model of the MOSFET including the breakdown network shown in Fig. 1(a) is employed to investigate reliability in the inductive breakdown region. Fig. 1(a) is a nonlinear model which is different from the linear small-signal equivalent circuit in Ref. [12]. The nonlinear model presented in this work is for the distortion analysis in the weak nonlinear region so that intrinsic nonlinear elements are introduced in Fig. 1(a). The physical origin of the RF avalanche breakdown mechanism can be referred to Ref. [12]. The bias-dependent nonlinear elements consist of the breakdown inductance L_{jd}, breakdown resistance R_{jd}, transconductance g_m, output conductance g_{ds}, gate-to-source capacitance C_{gs}, and gate-to-drain capacitance C_{gd}. C_{jd} is treated as a linear element in the presented Volterra analysis for simplicity because its nonlinear contribution is insignificant when compared with contributions from L_{jd} and R_{jd}. The extrinsic parameters are composed of parasitic resistances (R_g, R_d, R_s) and substrate network (C_{sub}, C_{bk}, R_{bk}). To evaluate device geometry dependence on nonlinear behavior, nMOSFETs with the different gate length (L_g), unit gate width (W_f), and total gate width ($W_f \times$ number of fingers N_f) fabricated by the 0.18 μm CMOS technology node from the Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan were employed. The layout diagram of different device geometry is shown in Fig. 1(b). It is noted that the same CMOS technology node where other device parameters such as the gate oxide thickness, junction depth, and doping concentration are fixed was employed so that the gate length dependence on nonlinear behavior can be evaluated fairly. Five different gate lengths were ranged from 0.18 to 0.5 μm comprising of 0.18 μm, 0.26 μm, 0.34 μm, 0.42 μm, and 0.5 μm at the fixed total gate width of 8 × 15 μm. The total gate width varied from 60 to 360 μm comprising of 4 × 15 μm, 8 × 15 μm, 8 × 30 μm, and 8 × 45 μm, and gate length was fixed at 0.18 μm. Three different unit gate widths were from 4 to 8 μm with the same total gate width of 8 × 15 μm and the same gate length of 0.18 μm.

The nonlinear model is obtained according to the multi-bias small-signal equivalent circuit. Scattering parameter (*S*-parameter) data of the MOSFETs is employed to establish the multi-bias small-signal equivalent circuit. *S*-parameters were measured by the Agilent microwave network analyzer E8364B from 0.4 to 26.5 GHz with the standard short–open–load–thru (SOLT) calibration [12,20] and the scalable de-embedding method [21] suitable for different-sized DUTs. Gate bias and drain bias were swept from 0.6 to 1.2 V and 1.6 to 2.8 V, respectively, which cover saturation and breakdown regions where the reliability issue is a concern to establish the model. Extrinsic elements were extracted using the curve fitting method [12] and then subtracted from de-embedded data. Afterward, the intrinsic parameters of the MOSFETs including L_{jd}, R_{jd}, C_{jd}, g_m, g_{ds}, C_{gs}, and C_{gd} were determined by fitting the de-embedded *S*-parameters through least square error function at multiple bias points [22]. Because the model parameters including the inductive network are extracted according to RF *S*-parameter measurements, determined Volterra kernels mentioned as follows can further consider the RF avalanche delay

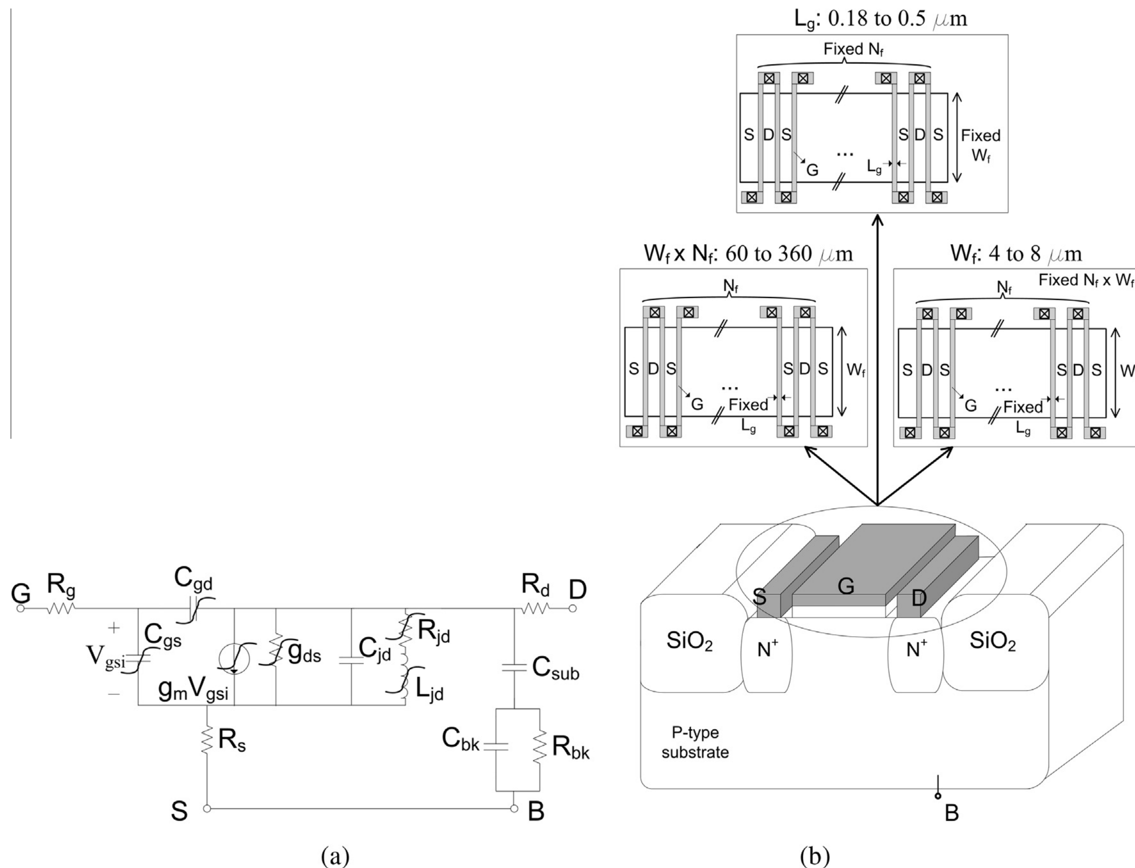

Fig. 1. (a) The nonlinear equivalent circuit model including the inductive breakdown network. (b) Cross section of the MOSFET and the layout diagram for different gate lengths, total widths, and unit widths.

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