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All-inkjet printed organic transistors: Dielectric surface passivation techniques for improved operational stability and lifetime

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ABSTRACT

We report about the use of a printed pentafluorothiophenol layer on top of the dielectric surface as a passivation coating to improve the operational stability of all-ink-jet printed transistors. Transistors with bottom-gate structure were fabricated using cross-linked poly-4-vinylphenol (c-PVP) as dielectric layer and an ink formulation of an amorphous triarylamine polymer as semiconductor. The resulting TFTs had low turn-on voltage (V_{th} < |5 V|) and a mobility ≈0.1 $cm^2/(V\,s)$. A comparison of identically fabricated transistors shows that devices with coated dielectric have a higher operational stability than those using bare c-PVP. This conclusion is supported by a quantitative study of the threshold voltage shift with time under continuous operation. Long exposure to the ambient atmosphere causes an increase in the threshold voltage strongly dependent on the used semiconducting ink formulation.

1. Introduction

Inkjet printing is a desirable manufacturing technology for low-cost, large-area and flexible organic electronic circuits. This fabrication technique uses a small amount of materials, it is a mask-less additive method and well-suited for applications that require heterogeneous integration of different materials and functional devices on the same substrate [1]. Organic-based Thin Film Transistors (OTFTs) entirely fabricated by inkjet have been reported [2–7]. Field effect mobility of 0.15 $cm^2/(V\,s)$, on/off ratio of 10^5 and inverter circuits with a voltage gain of almost −20 demonstrate that the technology is progressing [7]. This performance has been achieved by improving the dielectric/semiconductor interface using interlayers. For vacuum processed and spin-coated devices, hydrophobic coatings and self-assembled monolayers have been devised and optimized to prevent or neutralize traps on the dielectric surface.

For inkjet printed devices, this optimization is still in its infancy. The materials and process recipes developed in other deposition methods are not directly transferable to printing because they rely on complex procedures and reactions in inert atmosphere. Furthermore, the number of printing parameters to be optimized is higher and a clear understanding of how the printing process and materials affects the electrically active defects is still lacking.

In this contribution, the dielectric surface is coated with a printed pentafluorothiophenol (PFTP) layer. This molecule is commonly used to tune the energetic barrier at the metal/semiconductor interface [8]. Our findings suggest that it also neutralizes the traps on the dielectric surface. This coating improves the operational stability of the OTFT by one order of magnitude.

In addition to the operational stability, we also study the effects of ageing. OTFTs left for long periods of time to the ambient atmosphere undergo a decrease in the overall performance. This degradation is dependent on the semiconductor ink formulation. These results are discussed in terms of used solvents and their evaporation rates, which may affect the film morphology and their permeability to atmospheric species.

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2. Experimental details

A 125-μm-thick PEN film (Teijin DuPont Films, Teonex® Q65FA) was used as flexible substrate. Prior to printing, the PEN foil was cleaned with an ethanol impregnated clean-room wipe for some seconds. Then the cleaned foil was dried with nitrogen in order to remove remaining particles from the substrate. For printing, a Dimatix Materials Printer 2831 (DMP2831, Fujifilm Dimatix Inc.) was employed. The printer was equipped with 10 pL nominal drop volume printheads having 16 nozzles each with a diameter of about 21.5 μm. At first, the gate was deposited on the PEN substrate using 20% weight silver nanoparticle ink from Sunchemical (EMD5603). The deposited layer was sintered at 130 °C for 15 min on hotplate. The measured thickness of the resulting layer of the gate was about 450 nm. In the second step a solution of crosslinked poly-4-vinylphenol (c-PVP) was printed on top of the gate electrode and cross-linked at 150 °C for 40 min on a hotplate. The dielectric ink consisted of PVP (Mw ~ 25,000, Sigma Aldrich Co.) and poly(melamine-co-formaldehyde) (Mn ~ 432, 84 wt%, Sigma Aldrich Co.) as cross-linking agent that were mixed in propylene glycol monomethyl ether acetate (PGMEA). The dielectric layer thickness was about 1 μm. Next, interdigitated source–drain electrodes were printed using silver ink on top of the dielectric layer applying the same post-treatment described for the gate layer. For the deposition of the passivation layer, PFTP was dissolved in mesitylene at very low concentration. This ink formulation was printed on the pre-manufactured stack covering both the channel area and *S*/*D* fingers and exposed to ambient condition for some minutes. Finally, the organic semiconductor ink was deposited by using the same pattern of PFTP and cured on a heating plate at 100 °C for 15 min. The polymeric semiconductor inks were provided by Flexink and designated here as FS0027 and FS0096. FS0027 is triarylamine amorphous polymer dissolved in tetralin and the FS0096 is an ink formulation in mesitylene of a conjugated aromatic ordered polymer. Both semiconductors are p-type. The organic semiconductor was estimated to have a thickness of around 0.5 μm. Fig. 1(a) and (b) shows the layer-by-layer manufacturing process for the bottom gate bottom contact all-inkjet printed OTFTs. The OTFT device geometry was defined by the layout data of inkjet printing. The channel length (L) is 40 μm and channel width (W) is 4 cm. Fig. 1(c) shows the optical image of a printed OTFT based on the FS0096 ink. Electrical measurements were obtained using a Keithley 487 picoammeter/voltage source. All measurements were carried out in vacuum. For ageing studies, the OTFTs were stored in dark and ambient conditions.

3. Results and discussion

Fig. 2 shows typical output current–voltage (I–V) characteristics measured for OTFTs using the FS0027 ink formulation. From the transfer curve shown in Fig. 3a field effect mobility of 0.1 $cm^2/(V\,s)$ and a threshold voltage of 2.6 V are extracted from the slope and the intercept at voltage axis. The small departure from linearity at low gate–source voltages (V_{GS}) is due to a relatively high off-state drain–source current. This off-current is due to an undesirable current path. This feature is typical of an OTFT with a doped semiconductor.

The operational stability of the OTFT was assessed by measuring the time evolution of the threshold voltage shift $\Delta V_{th}(t)$ during the application of a constant gate voltage. This dependence is described by a stretched exponential function characterized by the parameters τ and β according to Eq. (1).

$$V_{th}(t) = V_{th0}\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \quad (1)$$

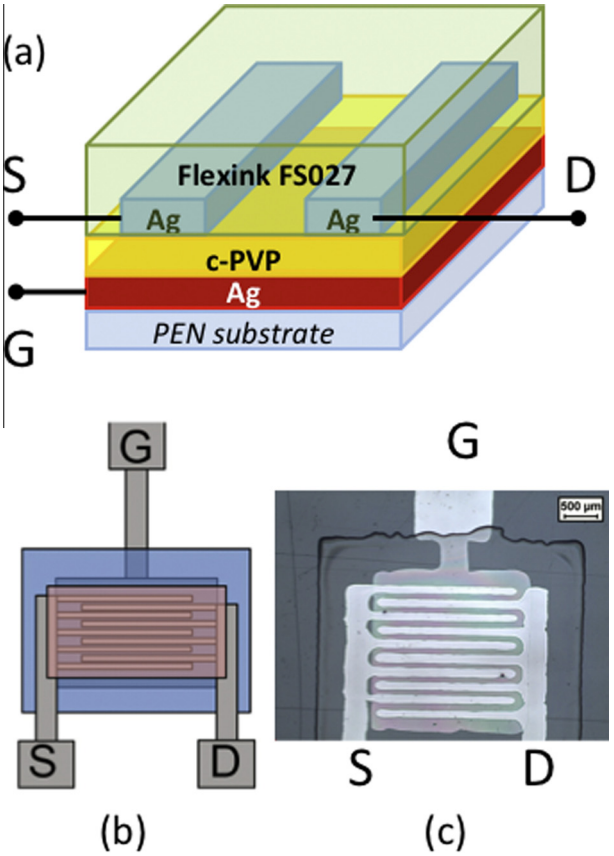

Fig. 1. (a) Schematic diagram showing the OTFT structure, (b) schematic diagram of the OTFT top view and (c) microscopic image of an inkjet printed OTFT on the flexible PEN substrate. The organic semiconductor (OSC) is the FS0096 ink formulation.

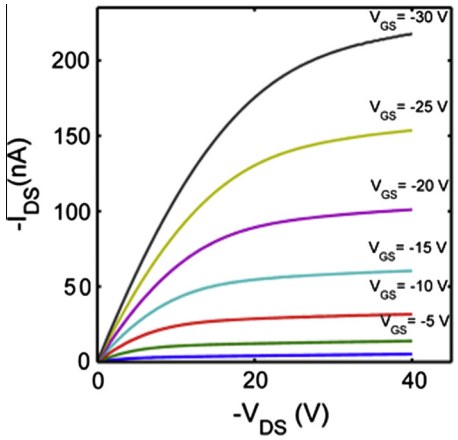

Fig. 2. Output current–voltage characteristics for an inkjet printed OTFT. The semiconductor used is FS0027.

where τ is a characteristic time constant and β a dispersion parameter, V_{th0} is the threshold voltage at the start of the experiment. The higher the value of τ, higher is the transistor operational stability, therefore τ is often used as a figure of merit to compare devices fabricated using different technologies [9].

Upon gate-bias stress the transfer curves shift in a parallel fashion, only the threshold voltage changes with stress time in agreement with our previous report [10]. Fig. 4 shows the time dependence of the threshold voltage shift for OTFTs having a non-coated and a PFTP-coated dielectric. The continuous line