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Interfacial reaction and failure mode analysis of the solder joints for flip-chip LED on ENIG and Cu-OSP surface finishes

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ABSTRACT

The interfacial reactions and failure modes of the solder joints for flip-chip light emitting diode (LED) on electroless nickel/immersion gold (ENIG) and Cu with organic solderability preservatives (Cu-OSP) surface finishes were investigated in this study. The experimental results demonstrate that the interfacial reactions in the Au/Sn–Ag–Cu(SAC)/ENIG and Au/SAC/Cu systems are different but the failure mechanisms of the two types of solder joints are similar during the shear test. For the Au/SAC/ENIG system, the Au layer on the surface finish of the diodes dissolved into the molten solder and transformed into a continuous (Au, Ni)Sn_4 IMC layer at the diode/solder interface during reflow and the interfacial IMC at the solder/ENIG interface is dendritic Ni_3Sn_4 IMC grains which are surrounded by (Au, Ni)Sn_4. For the Au/SAC/Cu system, however, no IMC layers can be observed at the diode/solder interface. The interfacial IMC at the solder/Cu interface is (Cu, Au)$_6Sn_5$ and a Cu_3Sn IMC layer at the (Cu, Au)$_6Sn_5$/Cu interface. Tiny (Au, Cu)Sn_4 IMC grains distribute in the solder layer and surround the (Cu, Au)$_6Sn_5$ grains. For the two types of systems, the primary failure mode for the cathode is due to the broken of the Si-based insulation layer which led to a high residue stress and poor connection between the Si-based layer and the solder layer. Meanwhile, the failure of the solder joint for the anode is mainly because of the failure of the solder layer under the conductive via. The crack generally forms at this area and then propagated along the diode or the diode/solder interface.

1. Introduction

Solid state lighting is considered as the dominated light source in the future, not only due to its high lumen efficiency, environmental friendly, and long life time over the traditional light source, but also benefited by its digital nature which enables its applications in smart lighting [1–3]. Currently, light emitting diode (LED) has been extensively used in various fields including indoor lamination, outdoor lighting, etc. [4–6]. The increasing requirements on the LED products promote the development of LED light source toward high power, high density, and low cost [7,8]. Therefore, flip-chip (FC) LED has been paid for more attention due to its higher heat dissipation, better light emission surface, higher reliability, and more efficiency bonding process than the traditional wire bond LED [9–11].

The typical bonding process recommended by the chip companies for the FC LED is Au/Sn eutectic bonding [12–14]. However, the high equipment cost and the low bonding efficiency of this process increase the manufacturing cost and thus suppress the batch production in industry. Additionally, misalignment may occur during the process and thus lead to an open or shot failure for the electronic circuit. In order to figure out this problem, soldering has been proposed as a candidate for the replacement of the Au/Sn eutectic bonding for FC LED packaging. For instance, the AuSn soldering process at 280–310 °C and the Sn–Ag–Cu (SAC) soldering at 250 °C [15–17]. Our previous study demonstrated that the defects such as large unbounded area, high residue stress, and reflectivity degradation of the substrates exist in the AuSn soldered FC LED packages. In contrast, such defects were not observed in the SAC soldered FC LED packages [18]. Although SAC soldering is considered as a promising method for FC LED packaging, further investigations are necessary for the improvement of this process.

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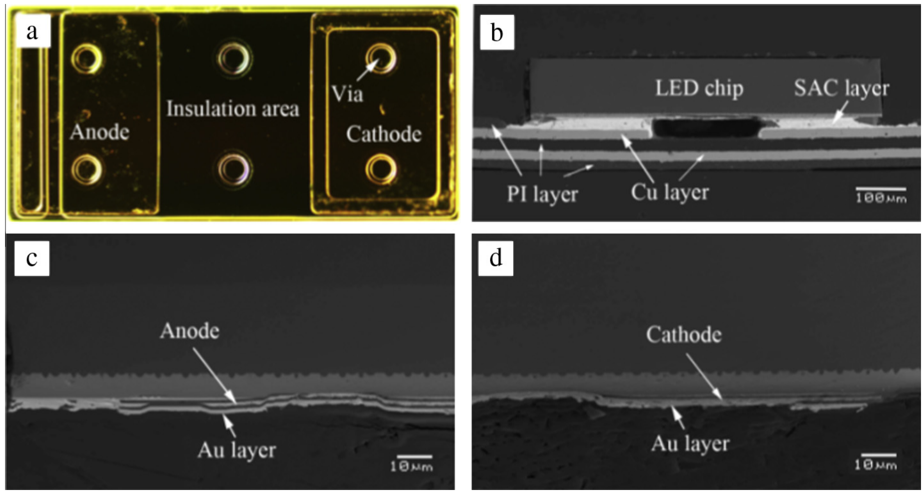

Fig. 1. Morphology and structure of the FC LED chip and package (a) the optical morphology of the electrodes, (b) the cross-sectional morphology of the LED package, (c) magnified view of the anode and (d) magnified view of the cathode.

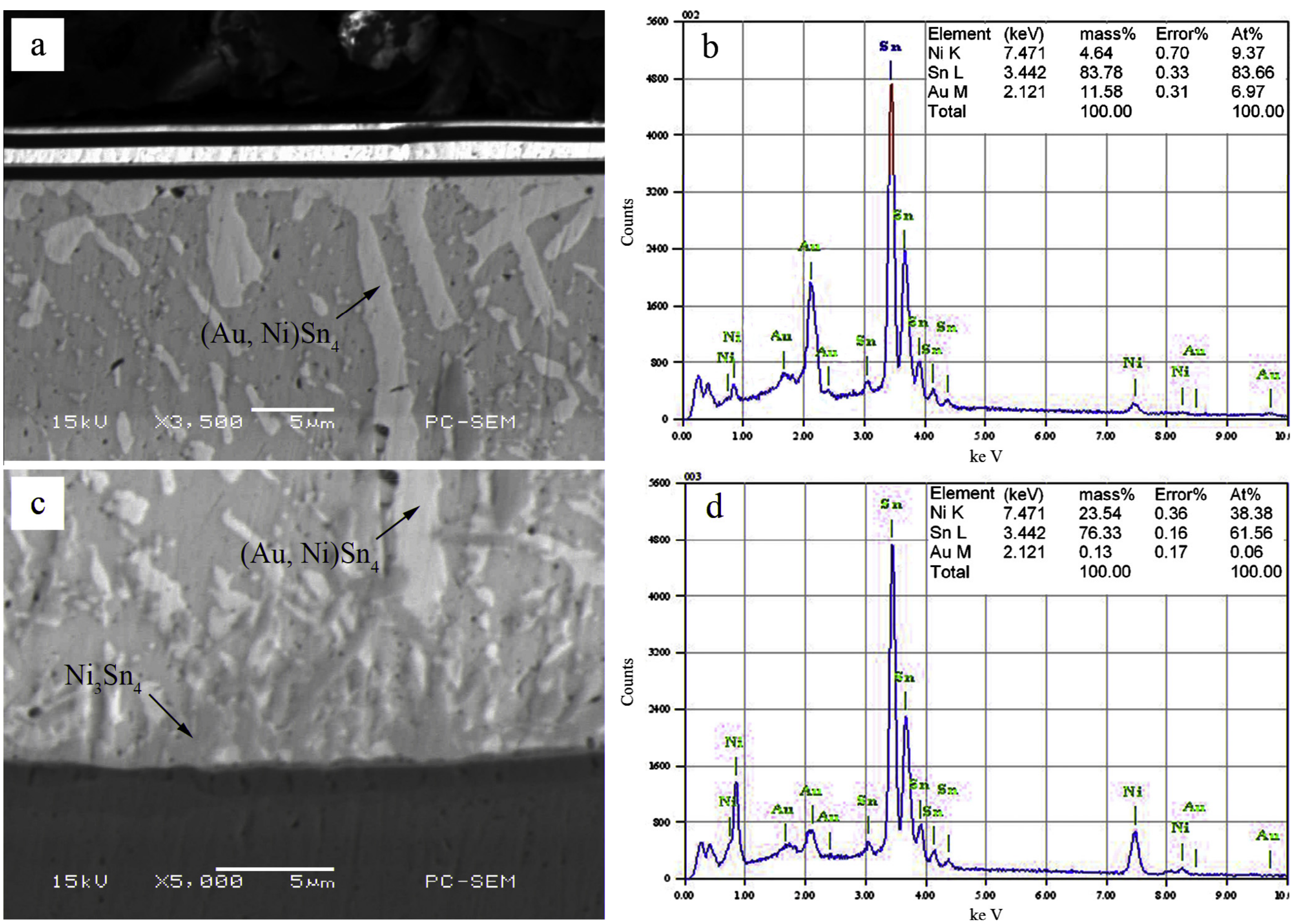

Fig. 2. The microstructure and EDS analysis of the solder joint on ENIG after reflow (a) the SEM cross-sectional morphology of the diode/solder interface, (b) EDS of (Au, Ni)Sn_4, (c) the SEM cross-sectional morphology of the solder/ENIG interface and (d) EDS of Ni_3Sn_4.

The FC LED chips with Au diodes were soldered to electroless nickel/immersion gold (ENIG) and Cu with organic solderability preservatives (Cu-OSP) surface finish, respectively by SAC soldering in this study. Although many researches have been conducted to the interfacial diffusions between SAC solder and substrates with ENIG or Cu-OSP surface finishes [19–23], limited literatures have reported relevant studies for LED solder joints. Because the Au layer at the diodes of the LED chips may have significant effects on the interfacial reactions between the solder layer and the surface finish layer of the substrates, it is necessary to investigate the interfacial reactions at the Au/SAC/Cu and Au/SAC/ENIG interfaces. Additionally, as one of the most important factors for the